(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 514 655 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **92105927.5**

(51) Int. Cl.5: **H03G 1/00**

(22) Date of filing: **06.04.92**

(30) Priority: **23.05.91 JP 118710/91**

(43) Date of publication of application:
25.11.92 Bulletin 92/48

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
1006, Oaza Kadoma
Kadoma-shi, Osaka-fu, 571(JP)

(72) Inventor: **Yagita, Hideki**
13-7, Kitafunahashicho
Hirakata-shi(JP)
Inventor: **Nakatsuka, Tadayoshi**
5-30, Daido-4-chome, Higashiyodogawa-ku
Osaka-shi(JP)

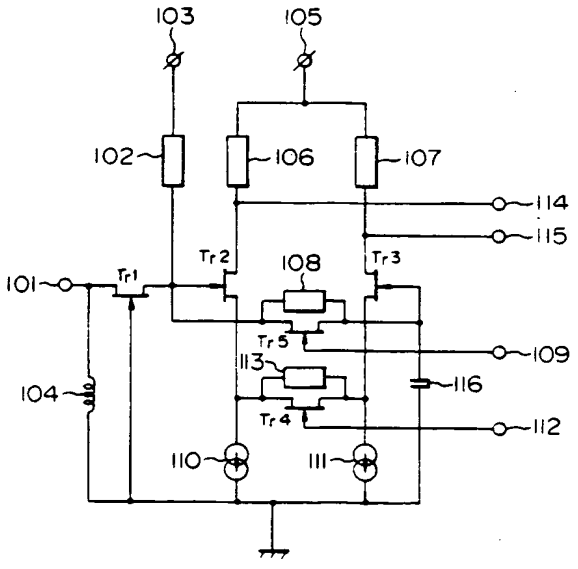
Inventor: **Kunihisa, Taketo**
17-11, Shimizucho
Neyagawa-shi(JP)
Inventor: **Tsuneoka, Michiaki**
13-12, Hiyoshidai Shichibancho
Takatsuki-shi(JP)
Inventor: **Sakai, Yukio**
70-182, Nojiricho
Sakai-shi(JP)
Inventor: **Yahata, Kazuhiro**
2-30, Oimazato-2-chome, Higashinari-ku
Osaka-shi(JP)

(74) Representative: **Graf von Wengersky, Anton**
Patentanwälte Leinweber & Zimmermann
Rosental 7
W-8000 München 2(DE)

(54) Semiconductor device for TV tuner and TV tuner using the same.

(57) This invention provides a semiconductor device for a tuner capable of simultaneously satisfying a low noise factor, low third order distortion characteristics and low power consumption, and a tuner using this semiconductor device for a tuner and capable of reducing the size and eliminating labor during assembly process. The semiconductor device for a tuner is a variable gain amplification circuit comprising a gate grounded circuit using a transistor (Tr1), and a differential amplification circuit including transistors (Tr2, Tr3) and constant current sources (110, 111). Transistors (Tr4, Tr5) are used as variable resistance devices, and the gain of the gate grounded circuit can be varied by changing the gate voltage of the transistor (Tr5). The gain of the differential amplification circuit can be varied by changing the gate voltage of the transistor (Tr4). The overall gain of the circuit can be varied within a necessary range by simultaneously operating these gain controls, and the third order distortion can be improved monotonously with the decrease of the gain.

FIG. 1



EP 0 514 655 A1

BACKGROUND OF THE INVENTION

This invention relates to a semiconductor device for a tuner for use in tuners of television receivers (hereinafter referred to as the "TV" tuners") for satellite broadcasting, having low noise, low third order distortion and moreover, low power consumption, and to such tuners.

Fig. 11 of the accompanying drawings shows a block diagram of a TV tuner circuit of the prior art which is an indoor TV tuner (so-called "BS tuner") for receiving satellite broadcasting, by way of example. In the drawing, reference numeral 1001 denotes an input terminal from an outdoor unit, 1002 is a band-pass filter, 1003 is a broad-band RF amplifier, 1004 is a variable attenuator, 1005 is a mixer circuit, 1006 a variable gain IF amplifier, 1007 is a band-pass filter, 1008 is an FM demodulator, 1009 is a video signal output terminal, 1010 is a buffer circuit for local oscillation signals, and 1012 is a phase-locked loop (PLL) circuit for stabilizing an oscillation frequency.

The intensity of input signal varies greatly in the TV tuner circuit depending on the condition of use. In the case of ordinary home use, the signal intensity is from -60 dBm to -40 dBm but in the case of a community receiving system, an input of about 0 dBm is sometimes inputted. In the case of the excessive input, third order distortion of mutually different channel signals enters the band and leads to cross modulation. Therefore, it is necessary to damp the excessive input signal and to prevent distortion of the video signals by the use of a variable attenuator and a variable gain amplifier, and the TV tuner must be all means secure a sufficient third order distortion suppression ratio for any input signal intensity.

In the prior art example shown in Fig. 11, a variable attenuator comprising the RF amplifier 1003 and a PIN diode and the variable gain IF amplifier 1006 are employed as the variable attenuator of the input circuit portion in order to prevent the excessive input. If the input signal is weak in this case, the damping factor of the variable attenuator 1004 is set to 0 dB and the broad band RF amplifier 1003 amplifies the signal. In this instance, the broad band RF amplifier 1003 must have a high noise factor. If the excessive input signal is inputted, on the other hand, the damping factor of the variable attenuator 1004 is set to -40 dB so as to prevent the excessive signal from being inputted to the mixer circuit 1005 but in this case, too, the excessive input signal is inputted to the RF amplifier 1003. For this reason, the RF amplifier 1003 must simultaneously possess excellent third order distortion characteristics and excellent cross modulation characteristics. In practice, however, the RF amplifier 1003 is used at an operation point at which current consumption is great, or a greater importance is set to only one of these characteristics, in order to simultaneously satisfy the low noise characteristics and the low third order distortion characteristics. These problems impede higher performance and lower power consumption of the tuner.

The prior art includes also a circuit which uses a variable gain RF amplifier using a dual gate FET shown in Fig. 12A to replace the variable attenuator 1004 comprising the PIN diode of Fig. 11. Fig. 12A shows a circuit example of the variable gain RF amplifier, and Fig. 12B shows a third order distortion suppression ratio (dBc, -20 dBm input) for the gain of this circuit and its consumed current (mA).

When this variable gain RF amplifier using the dual gate FET is employed, a wide gain variable width of 30 dB to 40 dB can be secured even in a single stage amplification circuit.

However, there are, on the other hand, various other problems. For example, the distortion characteristics cannot be improved even if the gain is lowered at the time of application of the excessive input signal because the input impedance changes with the change of the damping factor, because the third order distortion changes in a complicated way with the decrease of the gain as shown in Fig. 12B and moreover, because the third order distortion suppression ratio gets deteriorated with the decrease of the gain within the range of gain of 0 to 20 dB. Since Ids of the FET greatly changes with the change of the gain, it is difficult to keep the D.C. bias of the output by resistance load. Degradation of the third order distortion characteristics when the gain of the dual gate FET is lowered occurs because Ids is contracted by the second gate and the operation point enters the non-saturation region of the FET.

Furthermore, the conventional tuner circuit is produced by integrating discrete devices on a printed substrate. Therefore, the number of man-hours for assembly cannot be reduced when the tuner circuits are mass-produced, and since there are a large number of points which need adjustment, there are inevitable limits to the improvement in efficiency of the assembly process of the TV tuners and their scale-down.

According to the variable gain amplifier and the mixer circuit system of the prior art, it has been difficult to simultaneously satisfy the low noise factor, low third order distortion characteristics and low power consumption required for the TV tuners, and the reduction of the number of man-hours for the assembly and scale-down of the tuners have been difficult, as well.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor device for a tuner which can simultaneously satisfy a low noise factor, low third order distortion characteristics and low power consumption, and a tuner capable of reducing the size and the number of man-hours for assembly by the use of the semiconductor device for a tuner.

A semiconductor device for a tuner as defined in the appended Claim 1 includes a gate grounded circuit and a differential amplification circuit.

The gate grounded circuit uses the source electrode of a first FET as its input terminal, connects the drain electrode of the first FET to a first constant voltage source through a first load, and grounds the gate electrode of the first FET.

The differential amplification circuit connects the drain electrode of a second FET to a second constant voltage source through a second load, connects the source electrode of the second FET to a first constant current source, connects the drain electrode of a third FET to the second constant voltage source through a third load, connects further the source electrode of the third FET to a second constant current source, and also connects a fourth FET between the source electrode of the second FET and the source electrode of the third FET.

The drain electrode of the first FET of the gate grounded circuit and the gate electrode of the second FET of the differential amplification circuit are connected, and a fifth FET is interposed between the gate electrode of the second FET and the gate electrode of the third FET.

A semiconductor device for a tuner as defined in the appended Claim 2 includes a gate grounded circuit and a differential amplification circuit.

The gate grounded circuit uses the source electrode of a first FET as the input terminal, connects the drain electrode of the first FET to a first constant voltage source through a first load, connects a second FET in parallel with the first load, and grounds the gate electrode of the first FET.

The differential amplification circuit connects the drain electrode of a third FET to a second constant voltage source through a second load, connects the source electrode of the third FET to a constant current source, connects the drain electrode of a fourth FET to the second constant voltage source through a third load, further connects the source electrode of the fourth FET to the constant current source and connects a fifth FET between the drain electrode of the third FET and the drain electrode of the fourth FET.

The drain electrode of the first FET of the gate grounded circuit and the gate electrode of the third FET of the differential amplification circuit are connected, and a fourth load is interposed between the gate electrode of the third FET and the gate electrode of the fourth FET.

A semiconductor device for a tuner as defined in the appended Claim 3 includes a gate grounded circuit and a differential amplification circuit.

The gate grounded circuit uses the source electrode of a first FET as its input terminal, connects the drain electrode of the first FET to a first voltage source through a first load, connects a second FET in parallel with the first load, and grounds the gate electrode of the first FET.

The differential amplification circuit connects the drain electrode of a third FET to a second constant voltage source through a second load, connects the source electrode of the third FET to a first constant current source, connects the drain electrode of a fourth FET to the second constant voltage source through a third load, further connects the source electrode of the fourth FET to a second constant current source, and connects a fifth FET between the source electrode of the third FET and the source electrode of the fourth FET.

The drain electrode of the first FET of the gate grounded circuit and the gate electrode of the third FET of the differential amplification circuit are connected, and a fourth load is interposed between the gate electrode of the third FET and the gate electrode of the fourth FET.

A semiconductor device for a tuner as defined in the appended Claim 4 includes a gate grounded circuit, a differential amplification circuit and a double-balanced mixer circuit.

The gate grounded circuit uses the source electrode of a first FET as its input terminal, connects the drain electrode of the first FET to a constant voltage source through a first load, connects a second FET in parallel with the first load, and grounds the gate electrode of the first FET.

The differential amplification circuit connects the source electrode of a third FET to a first constant current source, connects the source electrode of a fourth FET to a second constant current source, and connects a fifth FET between the source electrode of the third FET and the source electrode of the fourth FET.

The double-balanced mixer circuit connects the drain electrode of a sixth FET and the drain electrode of a seventh FET to a constant voltage source, connects the drain electrode of an eight FET and the drain electrode of a ninth FET to the constant voltage source through a second load, connects the source electrode of the sixth FET to the source electrode of the eighth FET, connects the source electrode of the seventh FET to the source electrode of the ninth FET, uses the gate electrode of the sixth FET and the gate electrode of the ninth FET as a first input terminal of a local oscillation signal, and uses the gate electrode of

the seventh FET and the gate electrode of the eighth FET as a second input terminal of the local oscillation signal.

The drain electrode of the first FET of the gate grounded circuit is connected to the gate electrode of the third FET of the differential amplification circuit, the third load is interposed between the gate electrode of the third FET and the gate electrode of the fourth FET, the source electrodes of the sixth and eighth FETs are connected to the drain electrode of the third FET and the source electrodes of the seventh and ninth FETs are connected to the drain electrode of the fourth FET.

A semiconductor device for a tuner as defined in the appended Claim 5 includes a gate grounded circuit, a differential amplification circuit and a double-balanced mixer circuit.

The gate grounded circuit uses the source electrode of a first FET as its input terminal, connects the drain electrode of the first FET to a constant voltage source through a first load, connects a second FET in parallel with the first load and grounds the gate electrode of the first FET.

The differential amplification circuit connects the source electrode of a third FET to a constant current source, connects the source electrode of a fourth FET to the constant current source, and connects a fifth FET between the drain electrode of the third FET and the drain electrode of the fourth FET.

The double-balanced mixer circuit connects the drain electrodes of sixth and seventh FETs to the constant voltage source, connects the drain electrodes of eighth and ninth FETs to the constant voltage source through a second load, connects the source electrode of the sixth FET to the source electrode of the eighth FET, connects the source electrode of the seventh FET to the source electrode of the ninth FET, uses the gate electrodes of the sixth and ninth FETs as a first input terminal for a local oscillation signal, and uses the gate electrodes of the seventh and eighth FETs as a second input terminal of the local oscillation signal.

The drain electrode of the first FET of the gate grounded circuit is connected to the gate electrode of the third FET of the differential amplification circuit, the third load is interposed between the gate electrode of the third FET and the gate electrode of the fourth FET, connects the source electrodes of the sixth and eighth FETs to the drain electrode of the third FET, and connects the source electrodes of the seventh and ninth FETs to the drain electrode of the fourth FET.

A semiconductor device for a tuner as defined in the appended Claim 6 includes a gate grounded circuit, a differential amplification circuit and a double-balanced mixer circuit.

The gate grounded circuit uses the source electrode of a first FET as its input terminal, connects the drain electrode of the first FET to a constant voltage source through a first load, and grounds the gate electrode of the first FET.

The differential amplification circuit connects the source electrode of a second FET to a first constant current source, connects the source electrode of the third FET to a second constant current source, and connects a fourth FET between the source electrode of the second FET and the source electrode of the third FET.

The double-balanced mixer circuit connects the drain electrodes of fifth and sixth FETs to a constant voltage source, connects the drain electrodes of seventh and eighth FETs to the constant voltage source through a second load, connects the source electrode of the fifth FET to the source electrode of the seventh FET, connects the source electrode of the sixth FET to the source electrode of the eighth FET, uses the gate electrodes of the fifth and eighth FETs as a first input terminal of a local oscillation signal, and uses the gate electrodes of the sixth and seventh FETs as a second input terminal of the local oscillation signal.

The drain electrode of the first FET of the gate grounded circuit is connected to the gate electrode of the second FET of the differential amplification circuit, a ninth FET is interposed between the gate electrode of the second FET and the gate electrode of the third FET, connects the source electrodes of the fifth and seventh FETs to the drain electrode of the second FET, and connects the source electrodes of the sixth and eighth FETs to the drain electrode of the third FET.

A tuner as defined in the appended Claim 7 has a structure in which the semiconductor device for a tuner defined in the appended Claim 1, 2, 3, 4, 5 or 6 is mounted.

According to the structure of Claim 1, the fourth and fifth FETs are used as variable resistance devices, the gain of the gate grounded circuit can be changed by changing the gate voltage of the fifth FET, and the gain of the differential amplification circuit can be changed by changing the gate voltage of the fourth FET. Accordingly, the gain of the circuit can as a whole be changed within a necessary range by simultaneously operating the gain control by the fourth and fifth FETs. Moreover, since the currents flowing through the gate grounded circuit and the differential amplification circuit do not change D.C.-wise within the gain variable range, third order distortion characteristics can be improved monotonously with the decrease of the gain.

According to the structures of Claims 2 and 3, the second FET of the variable resistance device is used for the gain control of the gate grounded circuit and the fifth FET of the variable resistance

device is used for the gain control of the differential amplification circuit. The gain of the circuit can be changed as a whole within a necessary range by simultaneously operating the gain control by the second and fifth FETs. Moreover, since the currents flowing through the gate grounded circuit and the differential amplification circuit do not change D.C.-wise within the gain variable range, third order distortion characteristics can be improved monotonously with the decrease of the gain.

According to the structure of Claims 4 and 5, the second FET of the variable resistance device is used for the gain control of the gate grounded circuit and the fifth FET of the variable resistance device is used for the gain control of the differential amplification circuit. According to the structure of Claim 6, the ninth FET of the variable resistance device is used for the gain control of the gate grounded circuit and the fourth FET of the variable resistance device is used for the gain control of the differential amplification circuit. When the gain control by the FETs used as the variable resistance devices are simultaneously operated, the conversion gate of the circuit can be changed as a whole within a necessary range. Moreover, since the currents flowing through the gate grounded circuit and the differential amplification circuit do not change D.C.-wise within the gain variable range, third order distortion characteristics can be improved monotonously with the decrease of the conversion gain.

According to the structure of Claim 7, third order distortion characteristics can be improved monotonously with the decrease of the gain or the conversion gain by mounting the semiconductor device for a tuner defined in Claim 1, 2, 3, 4, 5 or 6.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram of a semiconductor device for a tuner according to a first embodiment of the present invention.

Fig. 2 is a circuit diagram of a semiconductor device for a tuner according to a second embodiment of the present invention.

Fig. 3 is a circuit diagram of a semiconductor device for a tuner according to a third embodiment of the present invention.

Fig. 4 is a diagram showing a suppression ratio of third order distortion to the gain of the semiconductor device for a tuner according to the first to third embodiments of the present invention and actually measured values of noise factors.

Fig. 5 is a circuit diagram of a semiconductor device for a tuner according to a fourth embodiment of the present invention.

Fig. 6 is a circuit diagram of a semiconductor device for a tuner according to a fifth embodiment of the present invention.

Fig. 7 is a circuit diagram of a semiconductor device for a tuner according to a sixth embodiment of the present invention.

Fig. 8 is a diagram showing a suppression ratio of third order distortion to the conversion gain of the semiconductor device for a tuner according to the fourth to sixth embodiments of the present invention and actually measured values of noise factors.

Fig. 9 is a circuit diagram of a variable conversion gain type mixer oscillator IC formed by integrating the semiconductor device for a tuner of the fourth embodiment, an LO oscillator and an LO buffer circuit on one chip.

Fig. 10 is a block diagram of a tuner according to one embodiment of the present invention.

Fig. 11 is a block diagram of a conventional TV tuner for satellite broadcasting.

Fig. 12A is a circuit diagram of a variable gain amplifier using a dual gate FET according to the prior art, and Fig. 12B is a diagram showing third order distortion characteristics to the gain of a variable gain amplification circuit using the dual gate FET shown in Fig. 12A and current consumption characteristics.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The first embodiment of the present invention will be explained with reference to Fig. 1. This embodiment corresponds to Claim 1.

Fig. 1 is a circuit diagram of the semiconductor device for a tuner according to the first embodiment of the present invention.

This semiconductor device for a tuner is a variable gain amplification circuit comprising a gate grounded circuit which uses a transistor Tr1 and a differential amplification circuit which includes transistors Tr2, Tr3 and constant current sources 110, 111.

The gate grounded circuit uses the source electrode of the transistor Tr1 (first FET) as its input terminal 101, connects the drain electrode to a constant voltage source 103 (first constant voltage source) through a load 102 (first load), and grounds the gate electrode. A choke coil 104 is connected as a source load of the transistor Tr1.

The differential amplification circuit connects the drain electrode of the transistor Tr2 (second FET) to the constant voltage source 105 (second constant voltage source) through a load 106 (second load,) connects the source electrode to the constant current source 110 (first constant current source), further connects the drain electrode of the transistor Tr3 (third FET) to the constant voltage source 105 through a load 107 (third load), con-

nects the source electrode to the constant current source 111 (second constant current source), and interposes a parallel circuit of a transistor Tr4 (fourth FET) and a fixed resistance 113 between the source electrode of the transistor Tr2 and the source electrode of the transistor Tr3.

The drain electrode of the transistor Tr1 of the gate grounded circuit and the gate electrode of the transistor Tr2 of the differential amplification circuit are connected to each other, and a parallel circuit of a transistor Tr5 (fifth FET) and a fixed resistance 108 is interposed between the gate electrode of the transistor Tr2 and the gate electrode of the transistor Tr3. Reference numerals 109 and 112 denote gate electrode terminals, 114 and 115 denote output terminals, and 116 does a capacitor for grounding high frequency-wise the gate potential of the transistor Tr3.

The conductance gm of the transistor Tr1 is 20 mS and its threshold voltage Vth is -0.4 V. The conductance gm is selected so that the input impedance is 50 Ω. Since the source load of the transistor Tr1 is the choke coil 104 of 500 mH, a 0 V bias is applied to its gate and a current of Idss = 8 mA always flows through the transistor Tr1. The drain load 102 of the transistor Tr1 is a 1 mH choke coil and is connected to the constant voltage source 103 of 3.0 V. Each of the transistor Tr2 and Tr3 has a conductance gm of 120 mS and a threshold voltage Vth of -0.4 V. The two constant current sources 110 and 111 are 24 mA constant current sources, and each of the drain loads 106 and 107 comprises a parallel circuit of a 1 mH choke coil and a 50 Ω resistance. The constant voltage source 105 of the differential amplification circuit is 6.0 V, and a capacitor 116 is 1000 pF.

The conductance gm of the transistor Tr4 used as the variable resistance device is 50 mS and the transistor can be varied within the range of 20 to 500 Ω by the gate bias. At this time, the fixed resistance 113 connected in parallel with the transistor Tr4 is 100 Ω and this resistance value decides the upper limit of the variable resistance value. Similarly, the transistor Tr5 used as the variable resistance device has a conductance gm of 70 mS, and can be varied within the range of 15 to 200 Ω. The fixed resistance 108 connected in parallel with this transistor decides the upper limit of the variable range of the resistance value by the transistor Tr5.

The operation of the circuit having the construction described above will now be explained.

In this circuit, since the source electrode of the transistor Tr1 is grounded through the choke coil 104, it is driven D.C.-wise by Idss of the transistor Tr1. Even when the load 102 is a pseudo-resistance load, the D.C. bias voltage of the drain of the transistor Tr1 is constant. The output load of the gate grounded circuit using the transistor Tr1 is determined by the drain load 102, the channel resistance of the transistor Tr5 and the parallel value of the input impedance of the transistor Tr2 and the fixed resistance 108 because the capacitance value of the capacitor 116 is great. However, the input impedance of the transistor Tr2 is sufficiently greater than others, and when the choke coil, etc., is used for the load 102, the output load is substantially determined by the parallel value of the fixed resistance 108 and the channel resistance value of the transistor Tr5. Therefore, the output load can be varied by changing the potential to be applied to the gate electrode terminal 109 of the transistor Tr5, and the gain of the gate grounded circuit can thus be varied. In this case, the channel resistance of the transistor Tr5 is about 500 Ω when the drain potential of the transistor Tr1 is Vd1, the threshold voltage Vth of the transistor Tr1 is -0.6 V, the height of the potential barrier of the Schottky gate is Vb and the potential of the gate electrode terminal 109 is Vd1 - Vth. The channel resistance of the transistor Tr5 can be made to be about 10 Ω when the potential of the gate electrode terminal 109 is Vd1 + Vb.

In the differential amplification circuit, the source electrodes of the transistors Tr2 and Tr3 are connected to the source and drain of the transistor Tr4, respectively, and the channel resistance of the transistor Tr4 is varied by the potential applied to the gate electrode terminal 112 in the same way as in the case of the transistor Tr5. When the channel resistance of the transistor Tr4 is low, the source potentials of the transistors Tr2 and Tr3 are equal to each other and the operation is effected at the maximum gain of the differential amplification circuit. When the channel resistance of the transistor Tr4 is high, a difference occurs between the source potential of the transistor Tr3 and that of the transistor Tr2, the source potential of the transistor Tr2 changes in the same phase with respect to the high frequency signal input of the gate electrode of the transistor Tr2, negative feedback is applied and the gain of the differential amplification circuit decreases.

The overall gain of this circuit is the sum of the gain of the gate grounded circuit and that of the differential amplification circuit. Since the gain of the gate grounded circuit is proportional to the parallel value of the transistor Tr5 and the fixed resistance 108, the gain is maximum at the upper limit value determined by the resistance value of the fixed resistance 108 or in other words, when the transistor Tr5 is OFF, and becomes minimum when the transistor Tr5 has the lowest resistance value. In the differential amplification circuit, on the other hand, the gain becomes maximum when the parallel value of the transistor Tr4 and the fixed

resistance 113 is minimum, that is, when the transistor Tr4 is ON, and becomes minimum at the maximum value determined by the fixed resistance 113, that is, when the transistor Tr4 is OFF. Accordingly, the overall gain of the circuit becomes maximum when the transistor Tr5 is OFF and moreover, when the transistor Tr4is ON, and the gain becomes minimum when the transistor Tr5 is ON with the transistor Tr4 being OFF. The gain can be varied within the range of these maximum gain and minimum gain.

As described above, this embodiment can vary the overall gain of the circuit within the range necessary for the tuner circuit by simultaneously operating the gain control of the gate grounded circuit and that of the differential amplification circuit. Moreover, the currents flowing through the gate grounded circuit and the differential amplification circuit do not change D.C.-wise within the gain variable range described above, so that the operating points of the transistors Tr1, Tr2 and Tr3 are constant and the input impedance does not at all change. This is important in the third order distortion characteristics of the circuit, too, and there does not occur the case where the operating point of the FET enters a non-linear range within the gain variable range, as has been observed in the prior art using the dual gate FET. For this reason, the third order distortion characteristics can be improved monotonously with the decrease of the gain.

The second embodiment of the present invention will be explained with reference to Fig. 2. This embodiment corresponds to Claim 2.

Fig. 2 is a circuit diagram of the semiconductor device for a tuner according to the second embodiment of the present invention.

This semiconductor device for a tuner is a variable gain amplification circuit comprising a gate grounded circuit which uses a transistor Tr6 and a differential amplification circuit which includes transistors Tr8 and Tr9 and a constant current source 210.

The gate grounded circuit uses the source electrode of the transistor Tr6 (first FET) as its input terminal 201, connects the drain electrode to a constant voltage source 202 (first constant voltage source) through a load 203 (first load), connects a transistor Tr7 (second FET) in parallel with the load 203, and grounds the gate electrode of the transistor Tr6. A choke coil 215 is connected as a source load of the transistor Tr6.

The differential amplification circuit connects the drain electrode of the transistor Tr8 (third FET) to a constant voltage source 205 (second constant voltage source) through a load 204 (second load), connects the source electrode to the constant current source 210, further connects the drain electrode of the transistor Tr9 (fourth FET) to the constant voltage source 205 through a load 206 (third load), connects the source electrode to the constant current source, and connects a parallel circuit of a transistor Tr10 (fifth FET) and a fixed resistance 207 between the drain electrode of the transistor Tr8 and the drain electrode of the transistor Tr9.

The drain electrode of the transistor Tr6 of the gate grounded circuit is connected to the gate electrode of the transistor Tr8 of the differential amplification circuit, and a load 208 (fourth load) is interposed between the gate electrode of the transistor Tr8 and the gate electrode of the transistor Tr9. Reference numerals 211 and 214 denote gate electrode terminals, 212 and 213 denote output terminals and 209 does a capacitor for grounding high frequency-wise the gate potential of the transistor Tr9.

The transistor Tr6 has a conductance gm of 20 mS and a threshold voltage Vth of -0.4 V. The conductance gm is selected so that the input impedance becomes 50 Ω. Since the source load of the transistor Tr6 is the choke coil 215 of 500 mH, a 0 V bias is applied to the gate and a current Idss = 8 mA always flows through this transistor Tr6. The drain load of the transistor Tr6 comprises a load 203 obtained by connecting in parallel a 1 mH choke coil and a 1 KΩ fixed resistance with each other and the transistor Tr7 a variable resistance device which is connected in parallel with the load 203. The transistor Tr6 is connected to a 3.0 V constant voltage source 202 through this drain load. Each of the transistors Tr8 and Tr9 has a conductance gm of 120 mS and a threshold voltage Vth of -0.4 V. The constant current source 210 is a 48 mA constant current source, and each of the drain loads 204 and 206 comprises a parallel circuit of a 1 mH choke coil and a 50 Ω resistance. The constant voltage source 205 of the differential amplification circuit is 6.0 V. The drains of the transistors Tr8 and Tr9 are connected to each other through a parallel circuit of the transistor Tr10 of the variable resistance device and the fixed resistance 207. The fixed resistance 207 is 10 KΩ and the capacitor 209 is 1000 pF.

The transistor Tr7 used as the variable resistance device has a conductance gm of 50 ms and can be varied within the range of 20 to 500 Ω by the gate bias. At this time, the 1 KΩ fixed resistance 202 connected in parallel with this transistor Tr7 decides the upper limit of the variable resistance value. Similarly, the transistor Tr10 used as the variable resistance device has a conductance gm of 70 mS and can be varied within the range of 15 to 200 Ω. The fixed resistance 207 connected in parallel with this transistor Tr10 decides the upper limit of the variable range of the resistance value

by the transistor Tr10.

In this second embodiment, the overall gain of the circuit is the sum of the gain of the gate grounded circuit and the gain of the differential amplification circuit. Since the gain of the gate grounded circuit is proportional to the parallel value of the transistor Tr7 and the load 203, it becomes maximum at the upper limit value decided by the fixed resistance value of the load 203, that is, when the transistor Tr7 is OFF, and becomes minimum when the transistor Tr7 has the lowest resistance value. On the other hand, in the differential amplification circuit, the gain becomes maximum when the parallel value of the transistor Tr10 and the fixed resistance 207 is the smallest, that is, when the transistor Tr10 is ON, and becomes minimum at the maximum value decided by the fixed resistance 207, that is, when the transistor Tr10 is OFF. Accordingly, when the transistor Tr7 is OFF and moreover, when the transistor Tr10 is ON, the overall gain of the circuit becomes maximum, and when the transistor Tr7 is ON with the transistor Tr10 being OFF, the overall gain becomes minimum. The gain can be varied within the range of this minimum gain and the maximum gain.

The third embodiment of the present invention will be explained with reference to Fig. 3. This embodiment corresponds to Claim 3.

Fig. 3 is a circuit diagram of the semiconductor device for a tuner according to the third embodiment of the present invention. This semiconductor device for a tuner is a variable gain amplification circuit comprising a gate grounded circuit which uses a transistor Tr15 and a differential amplification circuit which includes transistors Tr11 and Tr12 and constant current sources 310 and 311.

The gate grounded circuit uses the source electrode of the transistor Tr15 (first FET) as its input terminal 301, connects the drain electrode to the constant voltage source 304 (first constant voltage source) through a load 303 (first load), further connects the transistor Tr13 (second FET) in parallel with the load 303, and grounds the gate electrode of the transistor Tr15. A choke coil 302 is connected as the source load of the transistor Tr15.

The differential amplification circuit connects the drain electrode of the transistor Tr11 (third FET) to the constant voltage source 305 (second constant voltage source) through a load 306 (second load), connects the source electrode to the constant current source 310 (first constant current source), further connects the drain electrode of the transistor Tr12 (fourth FET) to the constant voltage source 305 through a load 307 (third load), connects the source electrode to the constant current source 311 (second constant current source), and interposes a parallel circuit of a transistor Tr14 (fifth FET) and a fixed resistance 309 between the source electrode of the transistor Tr11 and the source electrode of the transistor Tr12.

The drain electrode of the transistor Tr15 of the gate grounded circuit is connected to the gate electrode of the transistor Tr11 of the differential amplification circuit, and a load 308 (fourth load) is interposed between the gate electrode of the transistor Tr11 and the gate electrode of the transistor Tr12. Reference numerals 315 and 316 denote gate electrode terminals, 313 and 314 denote output terminals, and reference numeral 312 denotes a capacitor for grounding high frequency-wise the gate potential of the transistor Tr14.

The transistor Tr15 has a conductance gm of 20 mS and a threshold voltage Vth of -0.4 V. The conductance gm is selected so that the input impedance becomes 50 Ω. Since the source load of the transistor Tr15 is a 500 mH choke coil 302, a 0 V bias is applied to the gate and a current Idss = 8 mA always flows through the transistor Tr15. The drain load of the transistor Tr15 comprises a parallel load of a 1 mH choke coil and a 1 KΩ resistance, and the transistor Tr13 as the variable resistance device connected in parallel with the former. The drain of this transistor Tr15 is connected to a 3.0 V constant voltage source 304 through this drain load. Each of the transistors Tr11 and Tr12 has a conductance gm of 120 mS and a threshold voltage Vth of -0.4 V. Each of the two constant current sources 310, 311 is a 24 mA constant current source, and each of the drain loads 306, 307 comprises a parallel circuit of a 1 mH choke coil and a 50 Ω resistance. The constant voltage source 305 of the differential amplification circuit is 6.0 V. The fixed resistance 308 is 10 KΩ and the capacitor 312 is 1000 pF.

The transistor Tr13 used as the variable resistance device has a conductance gm of 50 mS and can be varied within the range of 20 to 500 Ω. The fixed resistance of the load 303 connected in parallel with the transistor Tr13 at this time is 1 KΩ, and this resistance value decides the upper limit of the variable resistance value. Similarly, the transistor Tr14 used as the variable resistance device has a conductance gm of 70 mS and can be varied within the range of 15 to 200 Ω. Similarly, the fixed resistance 309 connected in parallel decides the upper limit of the variable range of the resistance value of the transistor Tr14.

In this third embodiment, the overall gain of the circuit is the sum of the gain of the gate grounded circuit and the gain of the differential amplification circuit. Since the gain of the gate grounded circuit is proportional to the parallel value of the transistor Tr13 and the load 303, it becomes maximum at the upper limit value decided by the fixed resistance value of the load 303, that is, when the transistor

Tr13 is OFF, and is minimum when the transistor Tr13 has the smallest resistance value. On the other hand, the gain of the differential amplification circuit becomes maximum when the parallel value of the transistor Tr14 as the variable resistance device and the fixed resistance 309 is the smallest, that is, when the transistor Tr14 is ON, and becomes minimum at the greatest value decided by the fixed resistance 309, that is, when the transistor Tr14 is OFF. Therefore, the overall gain of the circuit becomes minimum when the transistor Tr13 is OFF and moreover, when the transistor Tr14 is ON, and becomes minimum when the transistor Tr13 is ON with the transistor Tr14 being OFF. The gain can be varied within the range of these minimum and maximum values.

The characteristics of the semiconductor device for a tuner, which has been explained in the foregoing first to third embodiments and which is the variable gain amplification circuit, will be explained with reference to Fig. 4.

Fig. 4 shows the suppression ratio of third order distortion with respect to the gain and the actually measured values of the noise factors. In this diagram, the abscissa represents the gain (dB) of the amplification circuit and the ordinate represents the suppression ratio (dBc) of the third order distortion and the noise factor (dB). Solid lines 401 and 404 in the diagram represent the suppression ratios of the third order distortion and the actually measured value in the first embodiment, respectively, dash lines 402 and 405 represent the suppression ratio of the third order distortion and the actually measured value of the noise factor in the second embodiment, and one-dot-chain lines 403 and 406 represent the suppression ratio of the third order distortion and the actually measured value of the noise factor in the third embodiment, respectively. Though some differences are observed in the suppression ratios of the third order distortion and the noise factors between these embodiments, these differences are believed to result from substrates used for measurement and evaluation.

The maximum gain of the respective amplification circuits are from 14.2 to 14.8 dB and the suppression ratios of the third order distortion and the noise factors at this time are 31 to 32 dBc and 2.5 to 3.0 dB, respectively. The minimum gains are from -5.0 to -4.8 dB and the suppression ratios of the third order distortion at this time are 64.5 to 66.6 dBc. Also, the noise factors at this time are 18.0 to 18.5 dB. Particularly, the third order distortion linearly decreases with a gradient of about 3 times with the decrease of the gain in the range of from about 5 to about 15 dB.

When the circuit which improves linearly the third order distortion to the decrease of the gain is used for a variable gain amplification circuit of a TV tuner, the gain is reduced at the time of the excessive input and at the same time, the third order distortion can be improved. Therefore, not only the saturation of the output signal but also the cross modulation necessary for the multi-channel TV tuner can be improved. It can thus be appreciated that the semiconductor devices for a tuner according to the first to third embodiments of the present invention are suitable as the variable gain amplification circuit of the TV tuner.

The fourth embodiment of the present invention will be explained with reference to Fig. 5. This embodiment corresponds to Claim 4.

Fig. 5 is a circuit diagram of the semiconductor device for a tuner according to the fourth embodiment of the present invention.

This semiconductor device for a tuner is a variable conversion gain mixer circuit obtained by connecting a gate grounded circuit which uses a transistor Tr27, an RF buffer circuit as a differential amplification circuit which includes transistors Tr22, Tr23 and transistors Tr25, Tr26 as a constant current source, and a double-balanced mixer circuit to one another.

The gate grounded circuit uses the source electrode of the transistor Tr27 (first FET) as an RF input terminal 514 (input terminal), connects the drain electrode of the transistor Tr27 to a constant voltage source 518 through a parallel circuit of a resistance load 502 and a coil 503 (first load), connects in parallel a transistor Tr17 (second FET) used as a variable resistance device to the first load (502, 503), and grounds the gate electrode of the transistor Tr27. Reference numeral 501 denotes a coil. A transistor Tr16 is an active load of the gate grounded circuit. When a parallel load of the transistor Tr17, the resistance load 502 and the coil 503 is connected in series with the transistor Tr16 as the active load, the gain can be varied by the variable load of the gate grounded circuit. Reference numeral 515 denotes an AGC terminal of the transistor Tr17 used as the variable resistance device.

The RF buffer circuit connects the source electrode of the transistor Tr22 (third FET) to the transistor Tr25 (first constant current source), connects the source electrode of the transistor Tr23 (fourth FET) to the transistor Tr26 (second constant current source), and interposes a parallel circuit of a transistor Tr24 (fifth FET) and a fixed resistance 511 between the source electrode of the transistor Tr22 and the source electrode of the transistor Tr23, forming thereby a differential amplification circuit. The transistor Tr24 is used as a variable resistance device, and the fixed resistance 511 connected in parallel with the transistor Tr24 decides the upper limit of the resistance value of the transistor Tr24.

The double-balanced mixer circuit connects the drain electrode of a transistor Tr18 (sixth FET) and the drain electrode of a transistor Tr19 (seventh FET) to a constant voltage source 518, connects the drain electrode of a transistor Tr20 (eighth FET) and the drain electrode of a transistor Tr21 (ninth FET) to the constant voltage source 518 through a drain load (second load) comprising a parallel circuit of a coil 507, a resistance 508 and a capacitor 509, connects the source electrode of the transistor Tr18 to the source electrode of the transistor Tr20, connects the source electrode of the transistor Tr19 to the source electrode of the transistor Tr21, uses the gate electrode of the transistor Tr18 and the gate electrode of the transistor Tr21 as a first input terminal 516 of a local oscillation signal, and uses the gate electrode of the transistor Tr19 and the gate electrode of the transistor Tr20 as a second input terminal 517 of the local oscillation signal. The parallel circuit of the coil 507, the resistance 508 and the capacitor 509 constitutes an LC resonance circuit so as to tune with an IF frequency. In this embodiment, parameters are so set as to resonate with 400 MHz. Reference numeral 519 denotes an IF output terminal.

A fixed resistance 510 (third load) is interposed between the gate electrode of the transistor Tr22 and the gate electrode of the transistor Tr23, and the connection between the double-balanced mixer circuit and the RF buffer circuit is established by connecting the source electrodes of the transistors Tr18, Tr20 to the drain electrode of the transistor Tr22, and connecting the source electrodes of the transistors Tr19, Tr20 to the drain electrode of the transistor Tr23. A capacitor 505 which connects the gate grounded circuit to the differential amplification circuit forms a peaking circuit in cooperation with the coil 503 connected to the drain of the transistor Tr27, so as to improve the frequency characteristics at the time of the high gain of the gate grounded circuit, etc.

The fifth embodiment of the present invention will be explained with reference to Fig. 6. This embodiment corresponds to Claim 5.

Fig. 6 is a circuit diagram of a semiconductor device for a tuner according to the fifth embodiment of the present invention.

The semiconductor device for a tuner is a variable conversion gain mixer circuit obtained by connecting a gate grounded circuit which uses a transistor Tr38, an RF buffer circuit as a differential amplification circuit which includes transistors Tr34, Tr35 and transistor Tr37 as a constant current source, and a double-balanced mixer circuit.

In the same way as in the fourth embodiment, the gate grounded circuit uses the source electrode of the transistor Tr38 (first FET) as an RF input terminal 605 (input terminal), connects the drain electrode of the transistor Tr38 to a constant voltage source 618 through a parallel circuit of a resistance load 606 and a coil 607 (first load), connects a transistor Tr29 (second FET) used as a variable resistance device in parallel with the first load (606, 607), and grounds the gate electrode of the transistor Tr38. Reference numeral 601 denotes a coil. A transistor Tr28 is an active load to the gate grounded circuit, and the gain is varied by varying the load of the gate grounded circuit by connecting the transistor Tr29 and the parallel load of the resistance load 606 and the coil 607 in series with the transistor Tr28 as the active load. Reference numeral 604 denotes an AGC terminal of transistor Tr29 which is used as a variable resistance device.

The RF buffer circuit is a differential amplification circuit which connects the source electrode of a transistor Tr34 (third FET) and the source electrode of a transistor Tr35 (fourth FET) to a transistor Tr37 (constant current source), and interposes a parallel circuit of a transistor 36 (fifth FET) and a fixed resistance 612 between the drain electrode of the transistor Tr34 and the drain electrode of the transistor Tr35. The transistor Tr36 is used as a variable resistance device and the fixed resistance 612 connected in parallel with this transistor Tr36 decides the upper limit of the resistance value of the transistor Tr36.

In the same way as in the fourth embodiment, the double-balanced mixer circuit connects the drain electrode of a transistor Tr30 (sixth FET) and the drain electrode of a transistor Tr31 (seventh FET) to the constant voltage source 618, connects the drain electrode of a transistor Tr32 (eighth FET) and the drain electrode of a transistor Tr33 (ninth FET) to the constant voltage source 618 through a drain load (second load) comprising a parallel circuit of a coil 609, a resistance 610 and a capacitor 611, connects the source electrode of the transistor Tr30 to the source electrode of the transistor Tr32, connects the source electrode of the transistor Tr31 to the source electrode of the transistor Tr33, uses the gate electrode of the transistor Tr33 and the gate electrode of the transistor Tr30 as a first input terminal 602 of a local oscillation signal, and uses the gate electrode of the transistor Tr31 and the gate electrode of the transistor Tr32 as a second input terminal 603 of the local oscillation signal. The parallel circuit of the coil 609, the resistance 610 and the capacitor 611 as the drain load constitute an LC resonance circuit and tune with an IF frequency. In this embodiment, parameters are set as to resonate with 400 MHz. Reference numeral 615 denotes an IF output terminal.

A fixed resistance 613 (third load) is interposed between the gate electrode of the transistor Tr34 and the gate electrode of the transistor Tr35, and

the connection between the double-balanced mixer circuit and the RF buffer circuit is established by connecting the source electrodes of the transistors Tr30, Tr32 to the drain electrode of the transistor Tr34 and connecting the source electrodes of the transistors Tr31, Tr33 to the drain electrode of the transistor Tr35. A capacitor 608 for connecting the source grounded circuit to the differential amplification circuit constitutes a peaking circuit in cooperation with the coil 607 which is connected to the drain of the transistor Tr38 and improves the frequency characteristics at the time of the high gain of the gate grounded circuit.

The sixth embodiment of the present invention will be explained with reference to Fig. 7. This embodiment corresponds to Claim 6.

Fig. 7 is a circuit diagram of the semiconductor device for a tuner according to the sixth embodiment of the present invention.

This semiconductor device for a tuner is a variable conversion gain mixer circuit which is obtained by connecting a gate grounded circuit using a transistor Tr50, a differential amplification circuit as an RF buffer circuit including transistors Tr44, Tr45 and transistors Tr48, Tr49 as a constant current source, and a double-balanced mixer circuit.

The gate grounded circuit uses the source electrode of transistor Tr50 (first FET) as its RF input terminal 705 (input terminal), connects the drain electrode of the transistor Tr50 to a constant voltage source 706 through a transistor Tr39 (first load), and grounds the gate electrode of the transistor Tr50. Reference numeral 701 denotes a coil, and transistor Tr39 as a drain load is an active load of the gate grounded circuit. However, an actual load impedance is determined by the parallel value of a transistor Tr46 (ninth FET) used as a variable resistance device, a parallel load of a resistance load 710 and a coil 717, and the active load by the transistor Tr39. Accordingly, the gain of the gate grounded circuit is varied by the AGC voltage applied to an AGC terminal 715 of the transistor Tr46.

The RF buffer circuit is à differential amplification circuit which connects the source electrode of the transistor Tr44 (second FET) to the transistor Tr48 (first constant current source), connects the source electrode of the transistor Tr45 (third FET) to the transistor Tr49 (second constant current source), and interposes a parallel circuit of a transistor Tr47 (fourth FET) and a fixed resistance 711 between the source electrode of the transistor Tr44 and the source electrode of the transistor Tr45. The transistor Tr47 is used as a variable resistance device, and the fixed resistance 711 connected in parallel with the transistor Tr47 decides the upper limit of the resistance value of the transistor Tr47.

The double-balanced mixer circuit connects the drain electrode of a transistor Tr40 (fifth FET) and the drain electrode of a transistor Tr41 (sixth FET) to the constant voltage source 706, connects the drain electrode of a transistor Tr42 (seventh FET) and the drain electrode of a transistor Tr43 (eighth FET) to the constant voltage source 706 through a drain load (second load) comprising the parallel circuit of a coil 707, a resistance 708 and a capacitor 709, connects the source electrode of the transistor Tr40 to the source electrode of the transistor Tr42, connects the source electrode of the transistor Tr41 to the source electrode of the transistor Tr43, uses the gate electrode of the transistor Tr40 and the gate electrode of the transistor Tr43 as a first input terminal 703 of a local oscillation signal, and uses the gate electrode of the transistor Tr41 and the gate electrode of the transistor Tr42 as a second input terminal 704 of the local oscillation circuit. The parallel circuit of the coil 707, the resistance 708 and the capacitor 709 constitutes an LC resonance circuit and tunes with an IF frequency. In this embodiment, parameters are so set as to resonate with 400 MHz. Reference numeral 714 represents an IF output terminal.

A transistor Tr46, a resistance load 710 and a coil 717 are connected in parallel between the gate electrode of the transistor Tr44 and the gate electrode of the transistor Tr45, and the connection between the double-balanced mixer circuit and the RF buffer circuit is established by connecting the source electrodes of the transistors Tr40, Tr42 to the drain electrode of the transistor Tr44 and connecting the source electrodes of the transistors Tr41, Tr43 to the drain electrode of the transistor Tr45. A capacitor 702 for connecting the gate grounded circuit with the differential amplification circuit forms a peaking circuit in cooperation with the coil interposed between the gates of the transistors Tr44, Tr45 and improves the frequency characteristics at the time of the high gain of the gate grounded circuit.

The characteristics of the semiconductor device for a tuner which has been explained by the fourth to sixth embodiments and a variable conversion gain mixer circuit will be explained with reference to Fig. 8.

Fig. 8 shows a suppression ratio of third order distortion with respect to the conversion gain and actually measured values of noise factors. In the diagram, the abscissa represents the conversion gain (dB) of the mixer circuit and the ordinate does the suppression ratio (dBc) of the third order distortion and the noise factor (dB). Solid lines 801 and 804 in the diagram represent the suppression ratio of the third order distortion and the actually measured value of the noise factor in the fourth embodiment, respectively, dash lines 802 and 805 represent the suppression ratio of the third order

distortion and the actually measured values of the noise factor in the fifth embodiment, respectively, and one-dot-chain lines 803 and 806 represent the suppression ratio of the third order distortion and the actually measured value of the noise factor, respectively, of the sixth embodiment. Though some differences of the suppression ratios of the third order distortion and the actually measured values are observed between these embodiment, the differences are believed to be a measurement error and the characteristics of each mixer circuit are believed substantially the same.

The maximum gain of each mixer circuit is 14.2 to 14.8 dB. At this time, the suppression ratio of the third order distortion is 31 to 32 dBc and the noise factor is 3.0 to 3.9 dB. The minimum conversion gain is -5.0 to -4.8 dB. At this time, the suppression ratio of the third order distortion is 64.5 to 66.5 dB and the noise factor is 17.5 to 18.0 dB. Particularly when the gain is within the range of about 5 to about 15 dB, the third order distortion decreases linearly with a gradient of about three times with respect to the decrease of the conversion gain.

When the mixer circuit, which characterizingly improves linearly the third order distortion with respect to the decrease of the conversion gain, is used for a TV tuner, it lowers the conversion gain at the time of the excessive input and at the same time, can improve the third order distortion. Accordingly, the mixer circuit can prevent not only the saturation of the output signal but also the cross modulation necessary for a multichannel TV tuner. It can thus be appreciated that the semiconductor devices for a tuner according to the fourth to sixth embodiments of the present invention are extremely suitable as the variable conversion gain mixer circuit for the TV tuner.

The seventh embodiment of the present invention will be explained with reference to the drawing. This embodiment corresponds to Claim 7.

Fig. 9 is a circuit diagram of a variable conversion gain mixer oscillator IC obtained by integrating the variable conversion gain mixer circuit as the semiconductor device for a tuner according to the fourth embodiment, an LO oscillator and an LO buffer circuit by the use of a GaAs semiconductor.

A transistor Tr69 is a gate grounded circuit, and reference numeral 935 denotes an input terminal. A transistor Tr67 is an active load, and reference numerals 937 and 938 denote a terminal for connecting a coil outside the IC. A transistor Tr68 is a variable resistance device, and reference numeral 936 denotes an AGC terminal of the gate grounded circuit.

The RF buffer circuit comprises transistors Tr62, Tr63 and transistors Tr65, Tr66 as a constant current source. A transistor Tr64 and a resistance device 922 are devices for variable gain, and reference numeral 934 denotes an AGC terminal for the RF buffer circuit.

The double-balanced mixer circuit comprises transistors Tr58, Tr59, Tr60 and Tr61. A capacitor 925 is integrated in order to improve frequency characteristics.

A transistor Tr70 is a transistor for the LO oscillation circuit and is connected to an external resonance circuit from terminals 927, 928 and 929. A transistor Tr51 is an output buffer circuit for guiding the LO signal to a PLL circuit, and reference numeral 931 denotes an output terminal. Transistors Tr52, Tr53 and Tr54 constitute a differential amplifier for converting the LO signal to a balance signal and at the same time, for amplifying it. Transistors Tr55, Tr56 and Tr57 constitute an LO buffer circuit for supplying the LO signal to the double-balanced mixer circuit. Reference numeral 940 denotes a power source terminal, 930 is a ground terminal, 932 and 933 are terminals for grounding A.C.-wise the circuit through the capacitor, 901 to 924 and 926 are resistances, 939 is a terminal and 941 is a capacitor. The lines connecting terminals 927 to 940 to one another correspond to the boundary of the circuit.

Fig. 10 shows a TV tuner for satellite broadcasting which has the variable conversion gain mixer oscillator IC shown in Fig. 9 mounted thereto. Reference numeral 1001 denotes an input terminal. In the case of satellite broadcasting, it is an input terminal of a broadcasting signal outputted from an outdoor device and having a first intermediate frequency of 950 to 1750 MHz. In Fig. 10, reference numeral 1000 denotes the variable conversion gain mixer oscillator IC shown in Fig. 9, 1001 is an input terminal, 1002 is band-pass filter, 1006 is a variable gain IF amplifier, 1007 is a band-pass filter of an IF frequency, and 1008 is an FM demodulator. Reference numeral 1012 denotes a phase-locked loop (PLL) circuit for stabilizing the LO frequency and 1009 is an output terminal of a video signal. Returning to Fig. 11, as described above, according to this embodiment, the RF amplifier 1003, variable attenuator 1004, mixer circuit 1005, local oscillation circuit (OSC) 1011 and LO buffer circuit 1010 in accordance with the structure of the conventional TV tuner are integrated into one chip and can be mounted as the variable conversion gain mixer oscillator IC shown in Fig. 10 to the TV tuner. As a result, the attenuator circuit which has been believed difficult to integrate by GaAs IC in the past can be equivalently integrated and moreover, the wasteful circuit arrangement of the prior art in which the signal is amplified by the broadband amplifier RF 1003 and is then damped by the variable attenuator 1004 can be eliminated. Furthermore, the size of the TV tuner for satellite broad-

casting can be reduced and moreover, the number of components can drastically be reduced.

Furthermore, the variable conversion gain mixer oscillator IC1000 including the semiconductor device for a tuner according to the fourth embodiment has excellent characteristics in that the third order distortion characteristics with respect to the conversion gain are linearly improved with the decrease of the conversion gain. As a result, the third order distortion suppression ratio of at least 60 dBc can be secured within the range of the input signal intensity of up to 0 dBm, and a high performance tuner having both low noise factor and low third order distortion characteristics can be accomplished.

The semiconductor device for a tuner according to the present invention can vary the overall gain of the circuit or the conversion gain within a necessary range by operating simultaneously the gain control by the FETs used as the variable resistance devices. Moreover, since the currents flowing through the gate grounded circuit and through the differential amplification circuit do not change D.C.-wise within the gain variable range, the third order distortion characteristics can be improved monotonously with the decrease of the gain or the conversion gain. As a result, the now noise factor, the low third order distortion characteristics and low power consumption can be satisfied simultaneously.

When the semiconductor device for a tuner according to the present invention is mounted, the tuner of the present invention can satisfy the low noise characteristics and low power consumption and can drastically reduce the number of components. Therefore, the tuner of the present invention can eliminate labor during the assembly process and can accomplish scale-down of the apparatus.

Claims

1. A semiconductor device for a tuner comprising:

   a gate grounded circuit using a source electrode of a first FET (Tr1) as an input terminal (101), connecting a drain electrode of said first FET to a first constant voltage source (103) through a first load (102) and grounding a gate electrode of said first FET (Tr1); and

   a differential amplification circuit connecting a drain electrode of a second FET (Tr2) to a second constant voltage source (105) through a second load (106), connecting the source electrode of said second FET to a first constant current source (110), connecting a drain electrode of a third FET (Tr3) to said second constant voltage source (105) through a third load (107), connecting a source electrode of said third FET (Tr3) to a second constant current source (111), and interposing a fourth FET (Tr4) between the source electrode of said second FET (Tr2) and the source electrode of said third FET (Tr3);

   wherein the drain electrode of said first FET (Tr1) of said gate grounded circuit is connected to the gate electrode of said second FET (Tr2) of said differential amplification circuit, and a fifth FET (Tr5) is interposed between the gate electrode of said second FET (Tr2) and the gate electrode of said third FET (Tr3).

2. A semiconductor device for a tuner comprising:

   a gate grounded circuit using a source electrode of a first FET (Tr6) as an input terminal (201), connecting a drain electrode of said first FET (Tr6) to a first constant voltage source (202) through a first load (203), connecting said second FET (Tr7) in parallel with said first load (203), and grounding a gate electrode of said first FET (Tr6); and

   a differential amplification circuit connecting a drain electrode of a third FET (Tr8) to a second constant voltage source (205) through a second load (204), connecting a source electrode of said third FET (Tr8) to a constant current source (210), connecting a drain electrode of a fourth FET (Tr9) to said second constant voltage source (205) through a third load (206), connecting a source electrode of said fourth FET (Tr9) to said constant current source (210), and interposing a fifth FET (Tr10) between the drain electrode of said third FET (Tr8) and the drain electrode of said fourth FET (Tr9);

   wherein the drain electrode of said first FET (Tr6) of said gate grounded circuit is connected to the gate electrode of said third FET (Tr8) of said differential amplification circuit, and a fourth load (208) is interposed between the gate electrode of said third FET (Tr8) and the gate electrode of said fourth FET (Tr9).

3. A semiconductor device for a tuner comprising:

   a gate grounded circuit using a source electrode of a first FET (Tr15) as an input terminal (301), connecting a drain electrode of said first FET (Tr15) to a first constant voltage source (304) through a first load (303), connecting a second FET (Tr13) in parallel with said first load (303), and grounding a gate electrode of said first FET (Tr15); and

   a differential amplification circuit connect-

ing a drain electrode of a third FET (Tr11) to a second constant voltage source (305) through a second load (306), connecting a source electrode of said third FET (Tr11) to a first constant current source (310), connecting the drain electrode of a fourth FET (Tr12) to said second constant voltage source (305) through a third load (307), and interposing a fifth FET (Tr14) between the source electrode of said third FET (Tr11) and the source electrode of said fourth FET (Tr12);

wherein the drain electrode of said first FET (Tr15) of said gate grounded circuit is connected to the gate electrode of said third FET (Tr11) of said differential amplification circuit, and a fourth load (308) is interposed between the gate electrode of said third FET (Tr11) and the gate electrode of said fourth FET (Tr12).

4. A semiconductor device for a tuner comprising:

a gate grounded circuit using a source electrode of a first FET (Tr27) as an input terminal (514), connecting a drain electrode of said first FET (Tr27) to a constant voltage source (518) through a first load (502, 503), connecting a second FET (Tr17) in parallel with said first load (502, 503), and grounding a gate electrode of said first FET (Tr27);

a differential amplification circuit connecting a source electrode of a third FET (Tr22) to a first constant current source (Tr25), connecting a source electrode of a fourth FET (Tr23) to a second constant current source (Tr26), and interposing a fifth FET (Tr24) between the source electrode of said third FET (Tr22) and the source electrode of said fourth FET (Tr23); and

a double-balanced mixer circuit connecting a drain electrode of a sixth FET (Tr18) and a drain electrode of a seventh FET (Tr19) to said constant voltage source (518), connecting a drain electrode of an eighth FET (Tr20) and a drain electrode of a ninth FET (Tr21) to said constant voltage source (518) through a second load (507, 508, 509), connecting the source electrode of said sixth FET (Tr18) to the source electrode of said eighth FET (Tr20), connecting the source electrode of said seventh FET (Tr19) to the source electrode of said ninth FET (Tr21), using the gate electrode of said sixth FET (Tr18) and the gate electrode of said ninth FET (Tr21) as a first input terminal (516) for a local oscillation signal, and using the gate electrode of said seventh FET (Tr19) and the gate electrode of said eighth FET (Tr20) as a second input terminal (517) of said local oscillation signal;

wherein the drain electrode of said first FET (Tr27) of said gate grounded electrode is connected to the gate electrode of said third FET (Tr22) of said differential amplification circuit, a third load (510) is interposed between the gate electrode of said third FET (Tr22) and the gate electrode of said fourth FET (Tr23), the source electrodes of said sixth and eighth FETs (Tr18, Tr20) are connected to the drain electrode of said third FET (Tr22), and the source electrodes of said seventh and ninth FETs (Tr19, Tr21) are connected to the drain electrode of said fourth FET (Tr23).

5. A semiconductor device for a tuner comprising:

a gate grounded circuit using a source electrode of a first FET (Tr38) as an input terminal (605), connecting a drain electrode of said first FET (Tr38) to a constant voltage source (618) through a first load (606, 607), connecting a second FET (Tr29) in parallel with said first load (606, 607), and grounding a gate electrode of said first FET (Tr38);

a differential amplification circuit connecting a source electrode of a third FET (Tr34) to a constant current source (Tr37), connecting a source electrode of a fourth FET (Tr35) to said constant current source (Tr37), and interposing a fifth FET (Tr36) between a drain electrode of said third FET (Tr34) and a drain electrode of said fourth FET (Tr35); and

a double-balanced mixer circuit connecting a drain electrode of a sixth FET (Tr30) and a drain electrode of a seventh FET (Tr31) to said constant voltage source (618), connecting a drain electrode of an eighth FET (Tr32) and a drain electrode of a ninth FET (Tr33) to said constant voltage source (618) through a second load (609, 610, 611), connecting the source electrode of said sixth FET (Tr30) to the source electrode of said eighth FET (Tr32), connecting the source electrode of said seventh FET (Tr31) to the source electrode of said ninth FET (Tr33), using the gate electrode of said sixth FET (Tr30) and the gate electrode of said ninth FET (Tr33) as a first input terminal (602) of a local oscillation signal, and using the gate electrode of said seventh FET (Tr31) and the gate electrode of said eighth FET (Tr32) as a second input terminal (603) of said local oscillation signal;

wherein the drain electrode of said first FET (Tr38) of said gate grounded circuit is connected to the gate electrode of said third FET (Tr34) of said differential amplification circuit, a third load (613) is interposed between

the gate electrode of said third FET (Tr34) and the gate electrode of said fourth FET (Tr35), the source electrodes of said sixth and eighth FETs (Tr30, Tr32) are connected to the drain electrode of said third FET (Tr34), and the source electrodes of said seventh and ninth FETs (Tr31, Tr33) are connected to the drain electrode of said fourth FET (Tr35).

6. A semiconductor device for a tuner comprising:

a gate grounded circuit using a source electrode of a first FET (Tr50) as an input terminal (705), connecting a drain electrode of said first FET (Tr50) to a constant voltage source (706) through a first load (Tr39), and grounding a gate electrode of said first FET (Tr50);

a differential amplification circuit connecting a source electrode of a second FET (Tr44) to a first constant current source (Tr48), connecting a source electrode of a third FET (Tr45) to a second constant current source (Tr49), and interposing a fourth FET (Tr47) between the source electrode of said second FET (Tr44) and the source electrode of said third FET (Tr45); and

a double-balanced mixed circuit connecting a drain electrode of a fifth FET (Tr40) and a drain electrode of a sixth FET (Tr41) to said constant voltage source (706), connecting a drain electrode of a seventh FET (Tr42) and a drain electrode of an eighth FET (Tr43) to said constant voltage source (706) through a second load (707, 708, 709), connecting the source electrode of said fifth FET (Tr40) to the source electrode of said seventh FET (Tr42), connecting the source electrode of said sixth FET (Tr41) to the source electrode of said eighth FET (Tr43), using the gate electrode of said fifth FET (Tr40) and the gate electrode of said eighth FET (Tr43) as a first input terminal (703) of a local oscillation signal, and using the gate electrode of said sixth FET (Tr41) and the gate electrode of said seventh FET (Tr42) as a second input terminal (704) of said local oscillation signal;

wherein the drain electrode of said first FET (Tr50) of said gate grounded circuit is connected to the gate electrode of said second FET (Tr44) of said differential amplification circuit, a ninth FET (Tr46) is interposed between the gate electrode of said second FET (Tr44) and the gate electrode of said third FET (Tr45), the source electrodes of said fifth and seventh FETs (Tr40, Tr42) are connected to the drain electrode of said second FET (Tr44), and the source electrodes of said sixth and eighth FETs (Tr41, Tr43) are connected to the drain electrode of said third FET (Tr45).

7. A tuner comprising said semiconductor device for a tuner according to any of Claims 1 through 6 mounted thereto.

FIG. 1

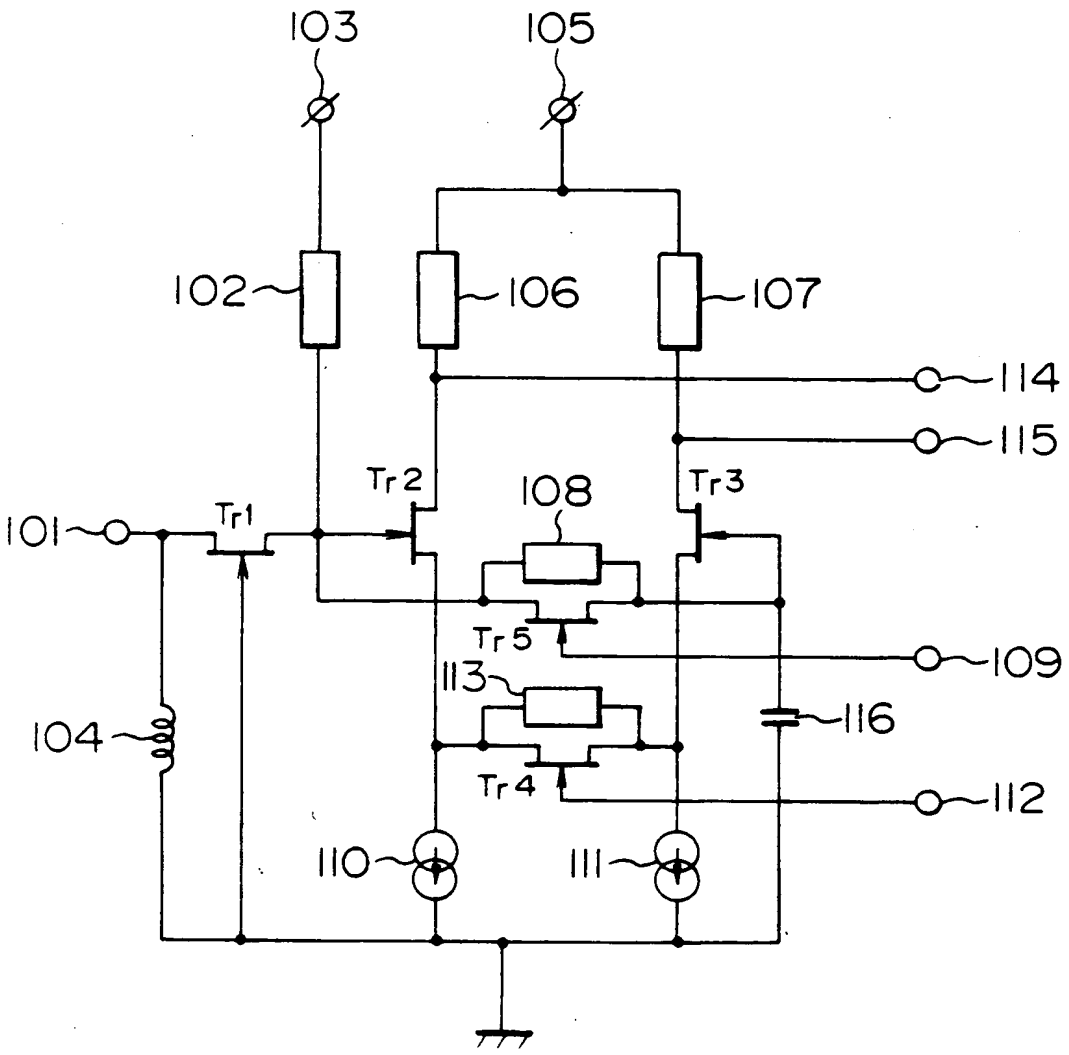


FIG. 2

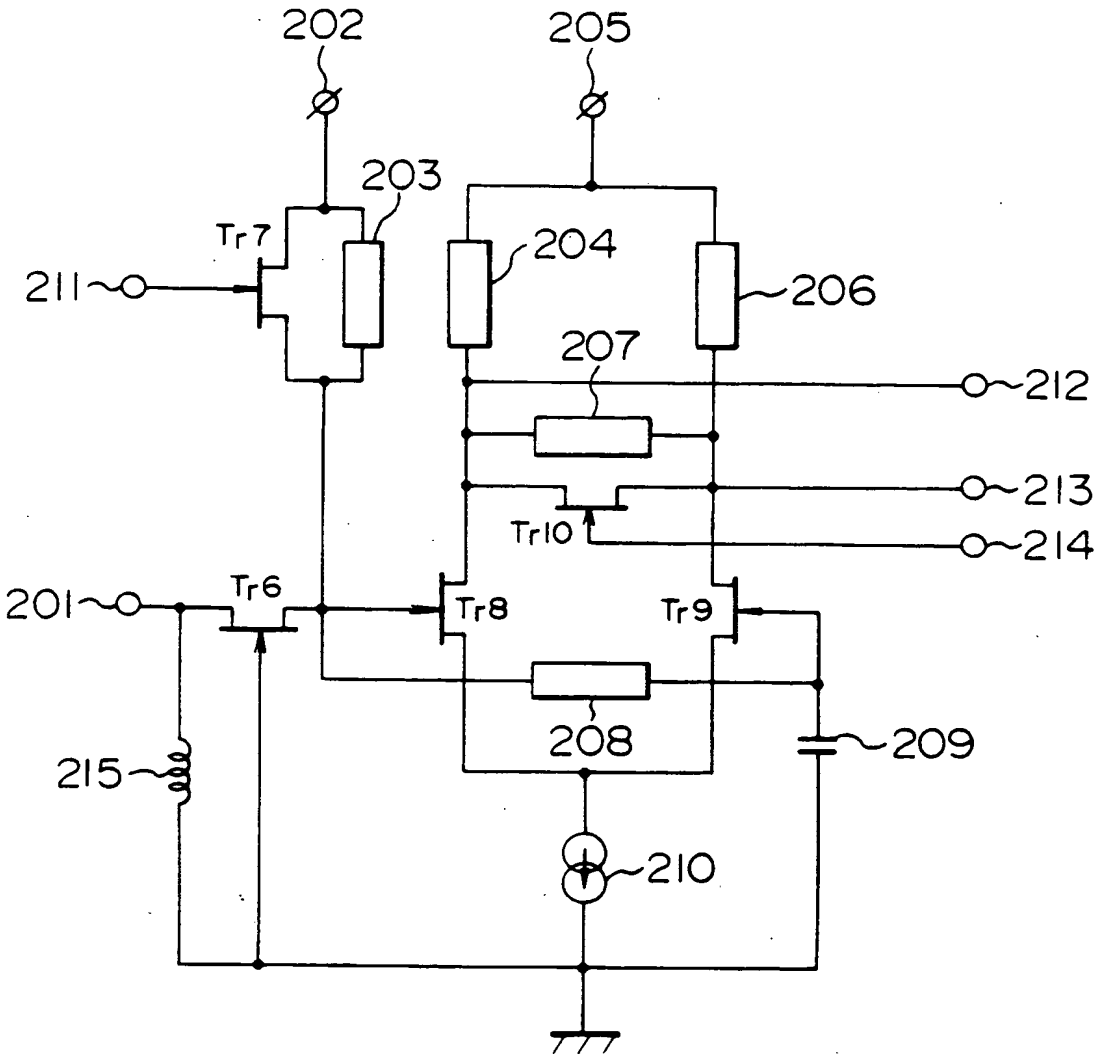


FIG. 3

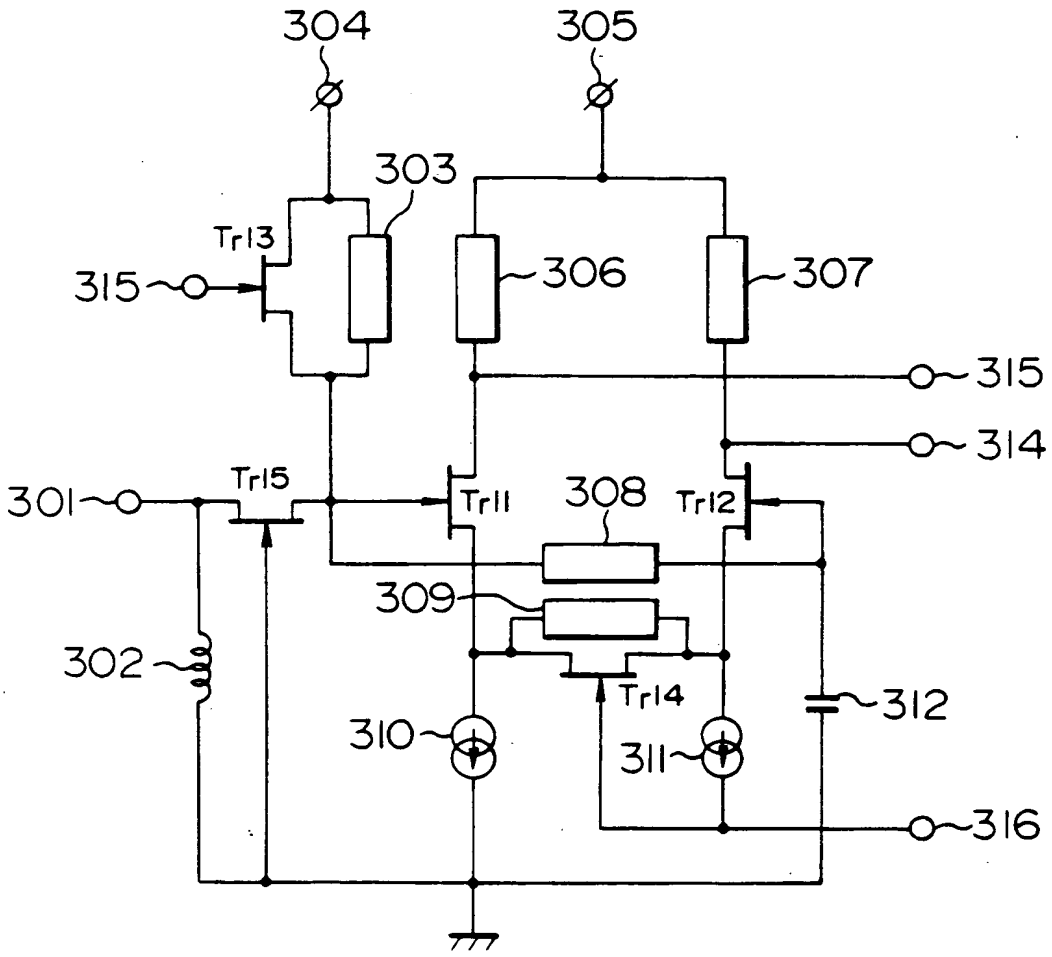

304
305
303
Tr13
315
306
307
315
314
301
Tr15
Tr11
308
Tr12
309
302
Tr14
312
310
311
316

FIG. 4

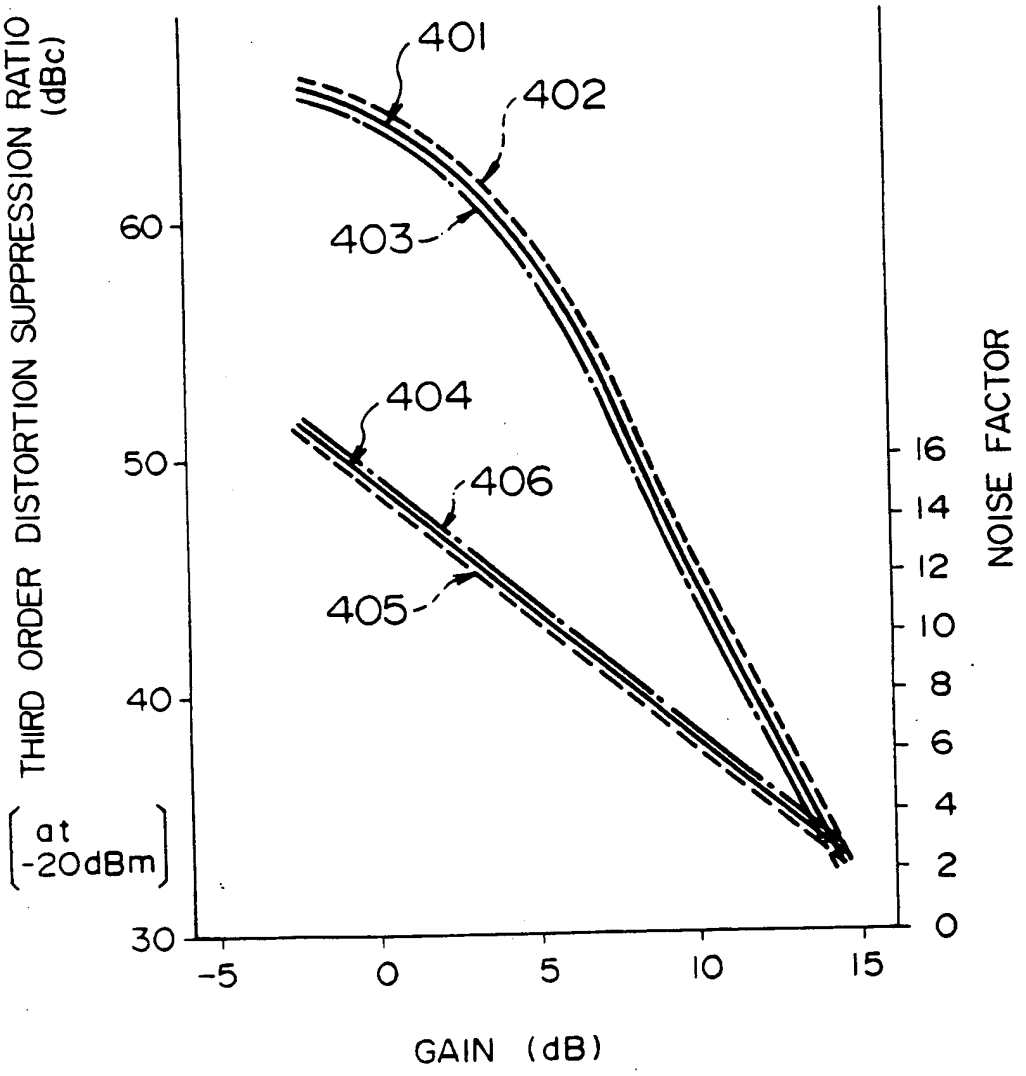


FIG. 5

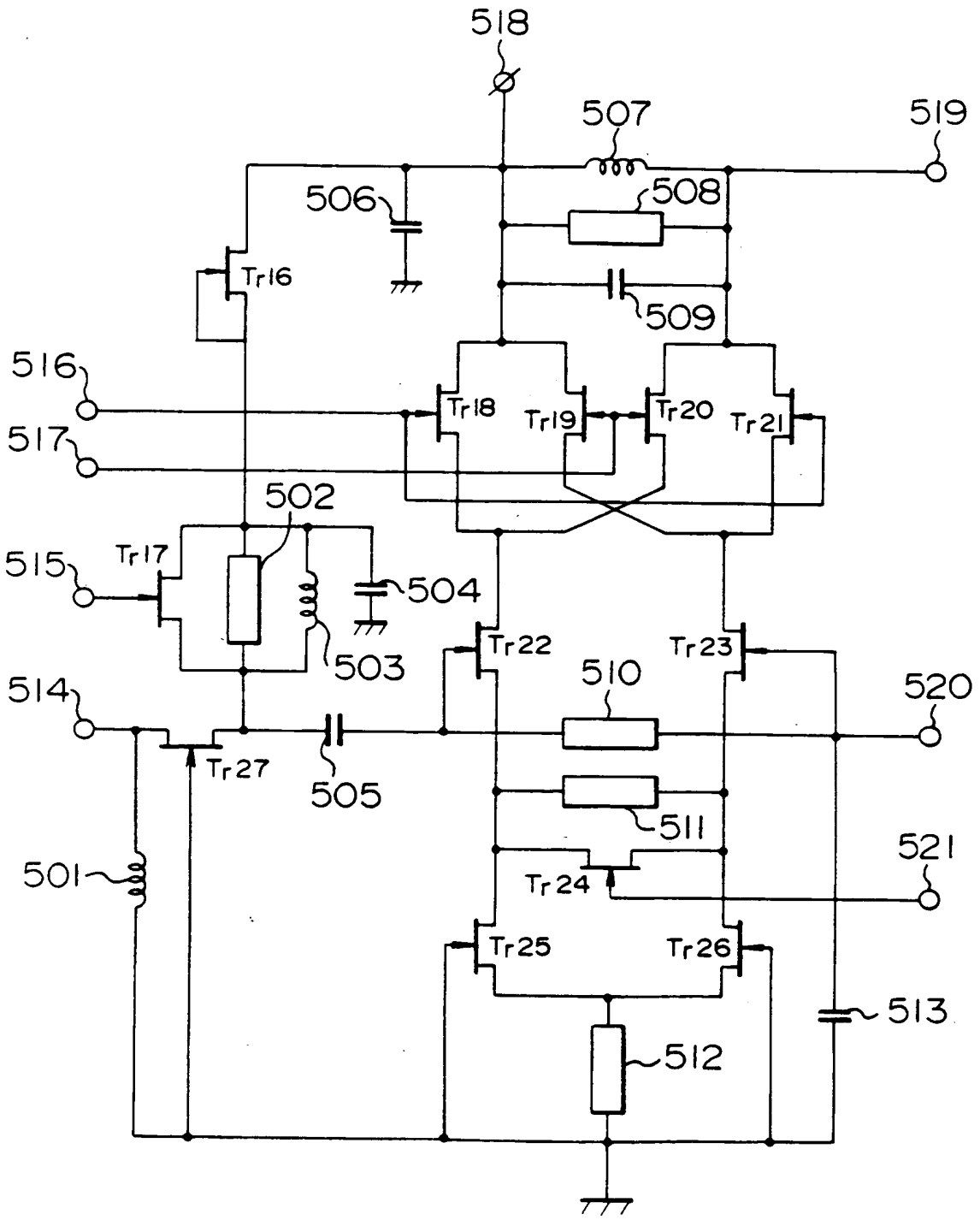


FIG. 6

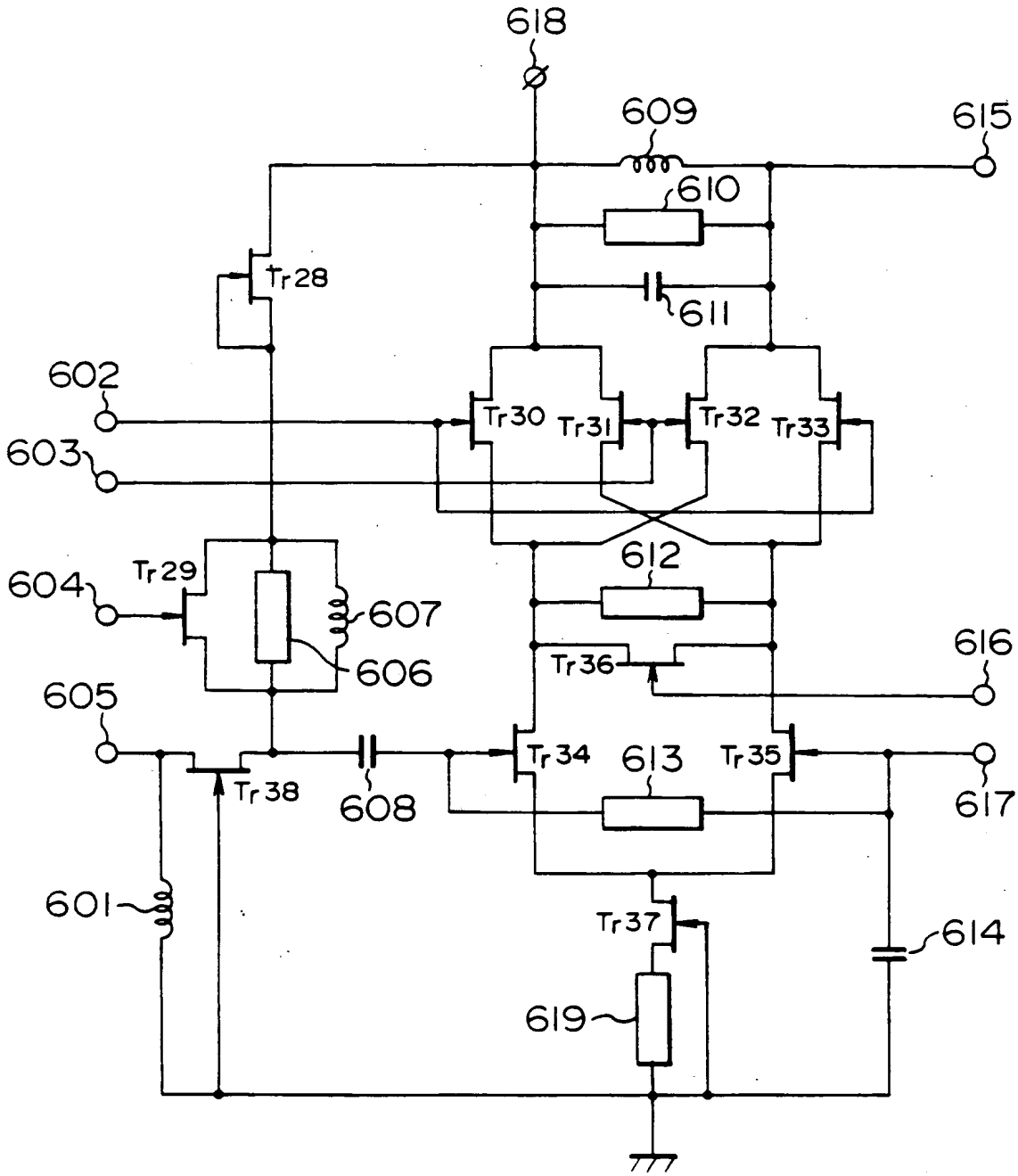

618
609
615
610
Tr28
611
602
603
Tr30
Tr31
Tr32
Tr33
612
604
Tr29
607
606
616
Tr36
605
Tr34
613
Tr35
617
Tr38
608
601
Tr37
614
619

FIG. 7

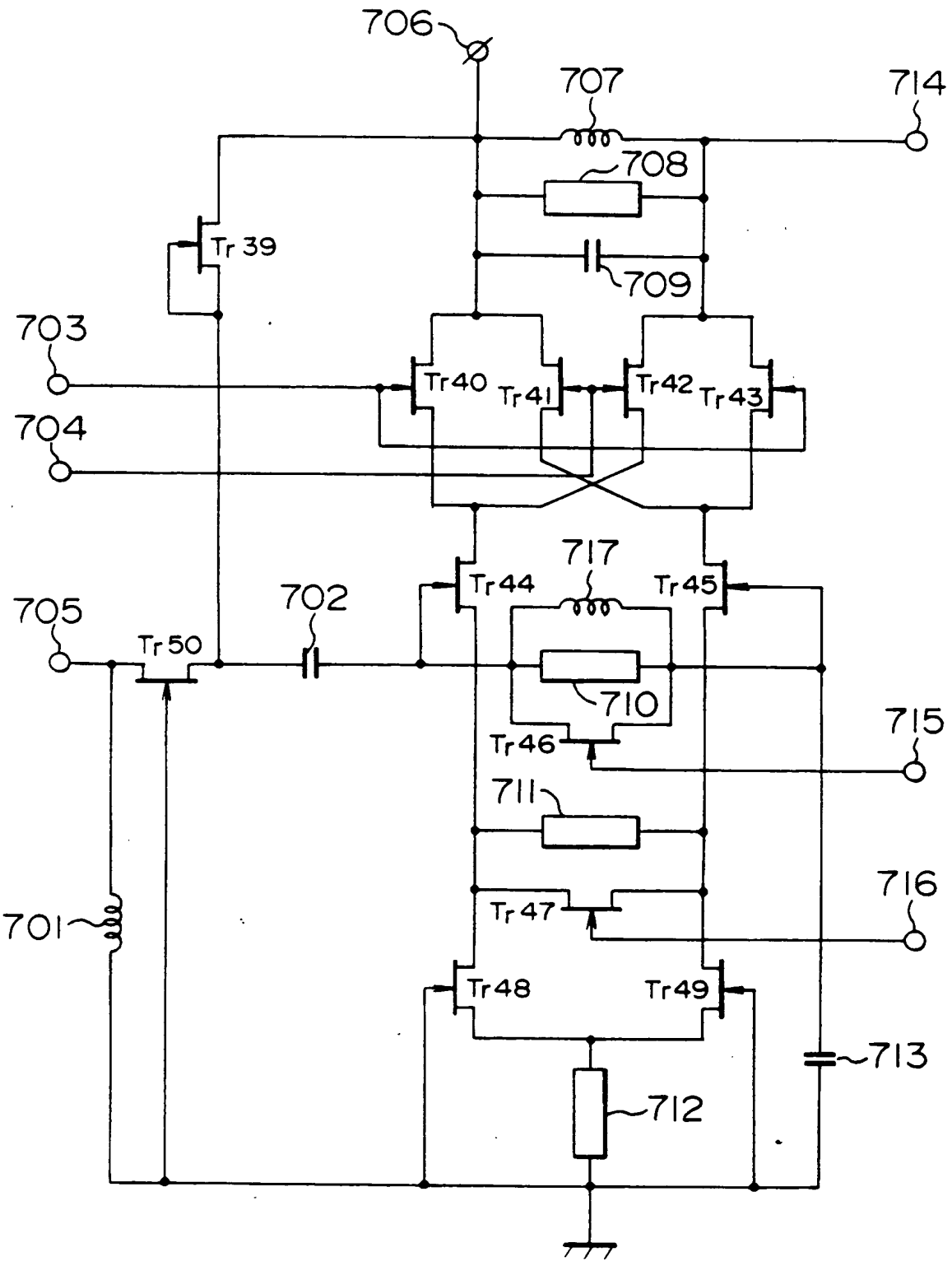


FIG. 8

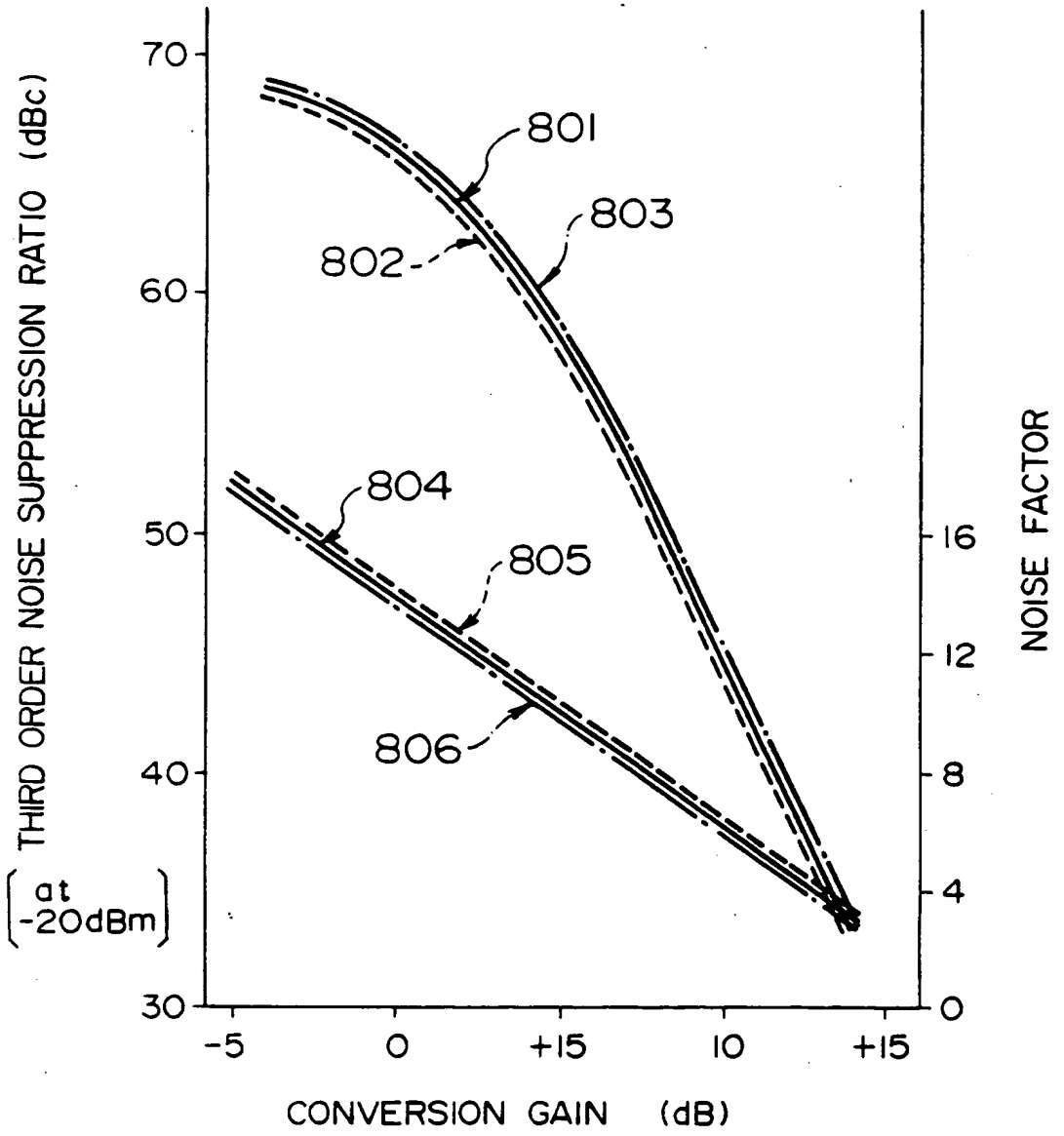


FIG. 9

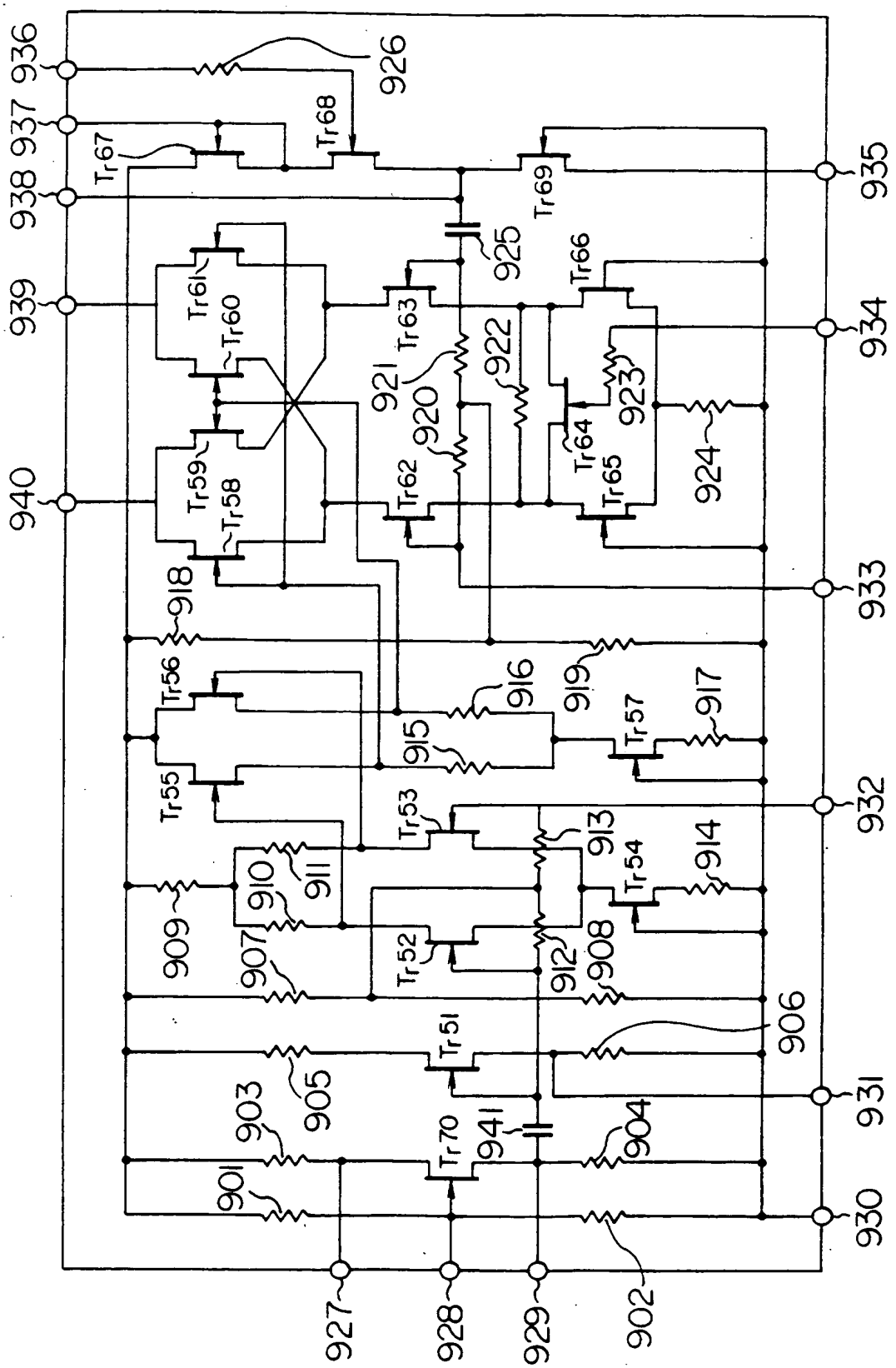

936
937
938
939
940
926
Tr67
Tr68
Tr69
935
925
Tr61
Tr60
Tr63
Tr66
934
921
922
923
920
Tr59
Tr58
Tr62
Tr64
Tr65
924
933
918
916
919
Tr56
Tr57
917
915
Tr55
Tr53
913
914
910
911
Tr54
909
907
Tr52
912
908
932
906
Tr51
905
903
931
941
904
Tr70
901
930
927
928
929
902

FIG. 10

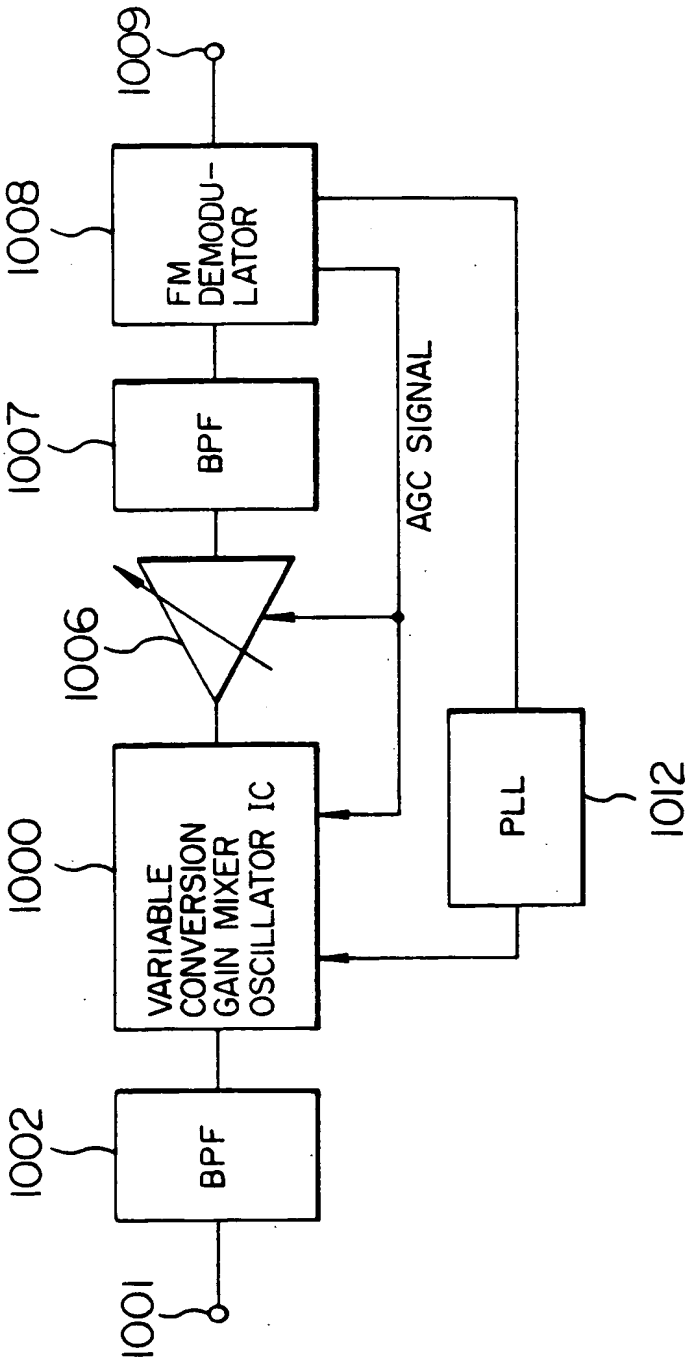


FIG. 11

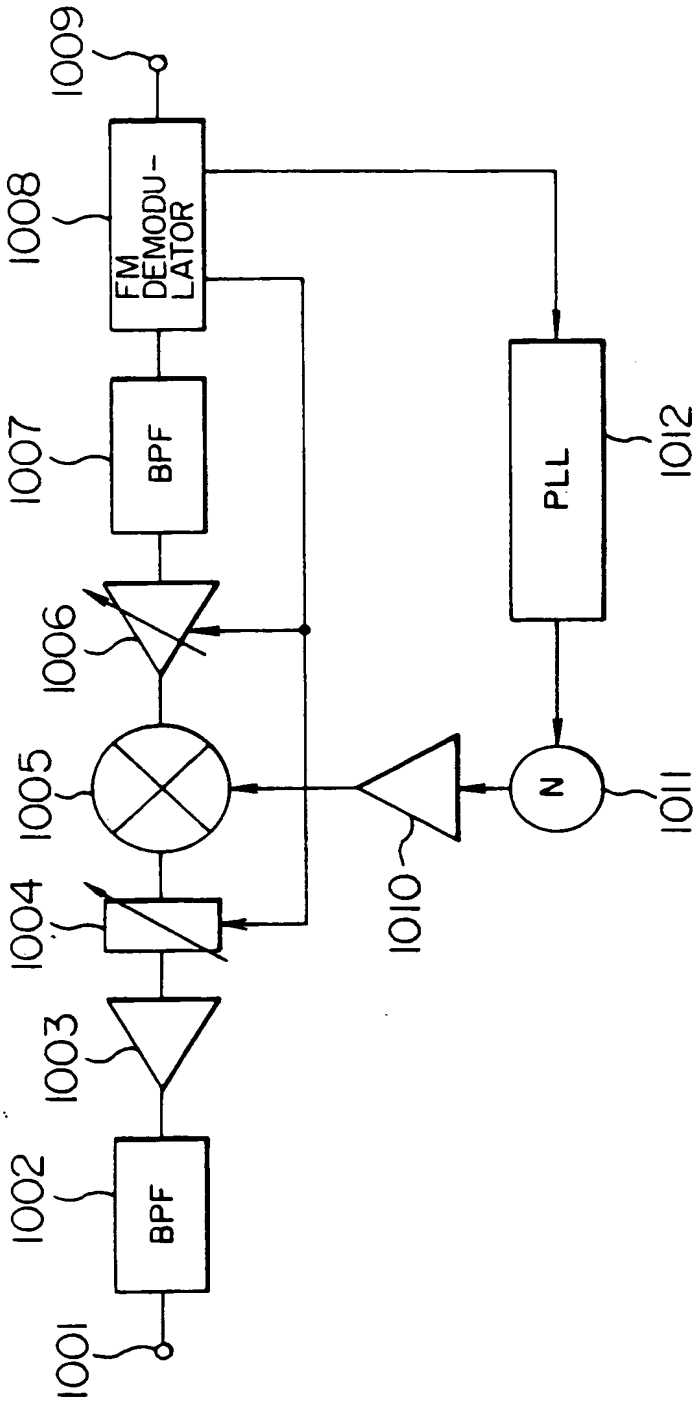


FIG. 12A

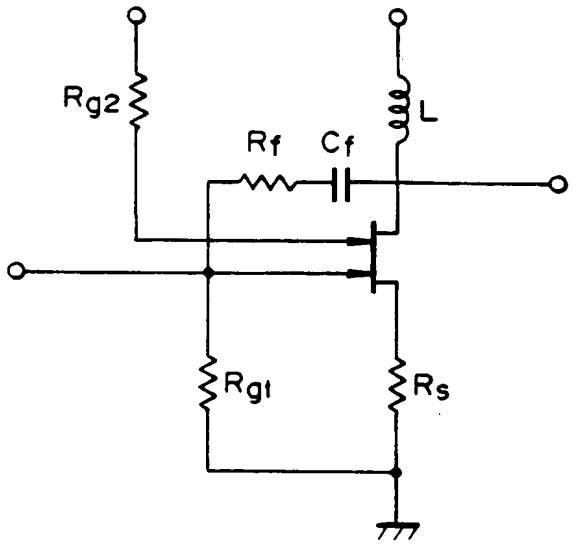
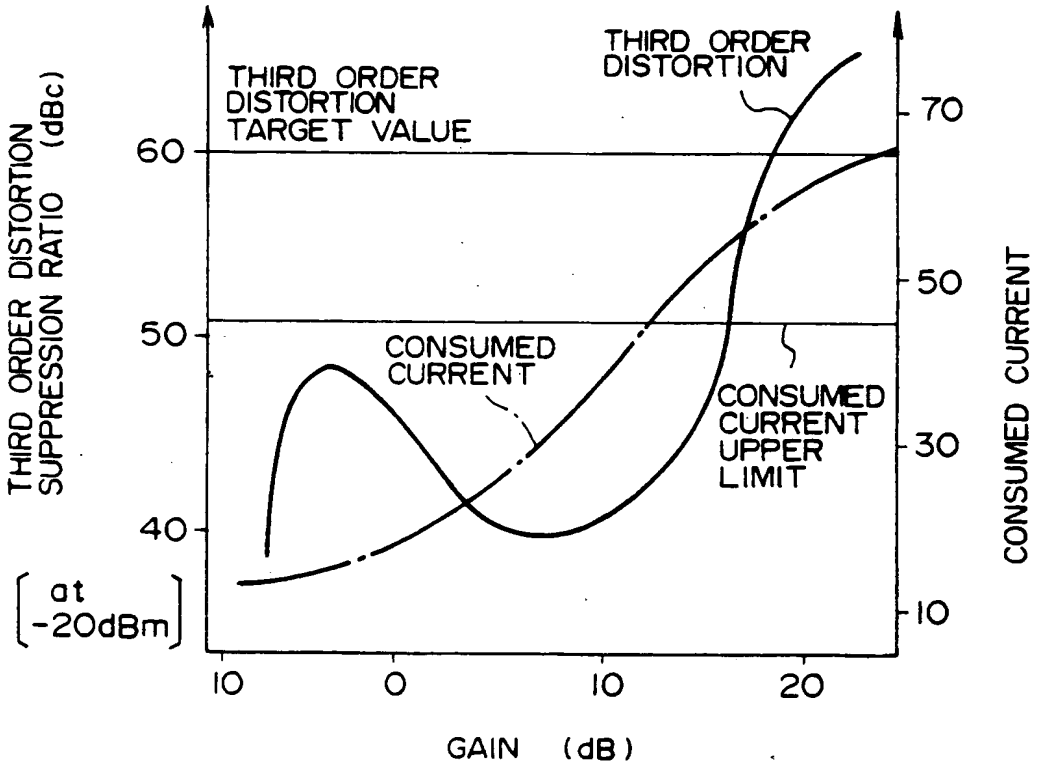


FIG. 12B



European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 10 5927

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-4 438 529 (TAKESHI SATO) * column 2, line 57 - column 3, line 5; figure 4 * ---	1-7	H03G1/00
A	PATENT ABSTRACTS OF JAPAN vol. 9, no. 201 (E-336)(1924) 17 August 1985 & JP-A-60 066 510 (NIPPON DENKI K. K.) 16 April 1985 * abstract * ---	1-6	
A	IBM TECHNICAL DISCLOSURE BULLETIN vol. 29, no. 11, 1 April 1987, ARMONK, NY, USA page 4840; 'BIFET VARIABLE GAIN AMPLIFIER' *FIGURE* * page 4840, line 5 - line 20 * -----	1-6	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H03G
H03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	25 JUNE 1992	BUTLER N.A.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)